

**Technical Explanation**  
**SEMITOP®**  
**Classic**

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## Revision History

SEMIKRON reserves the right to make changes without further notice herein

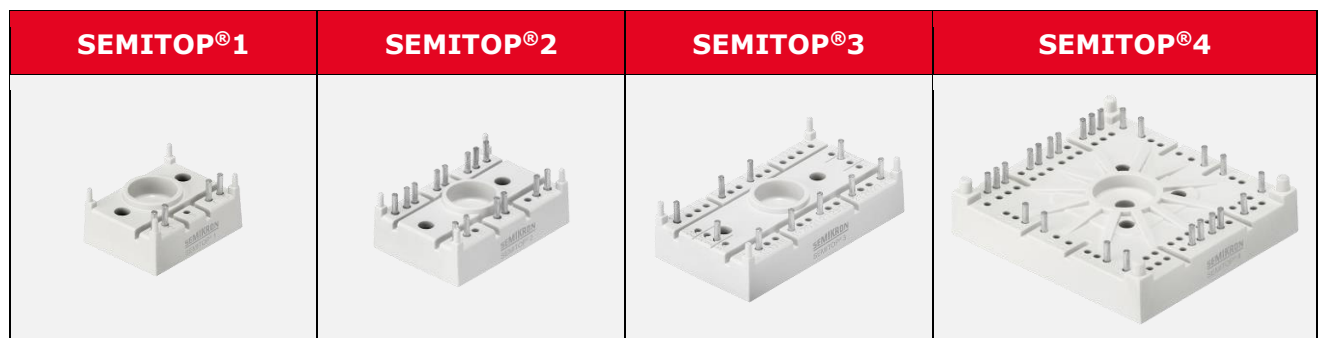
Date	Revision n°	Description	Pages
14.10.2015	03	Update of contents; Introduction of the new template.	65
31.07.2017	04	General review; Update of Mounting specifications for SEMITOP® (Table 21).	65
28.08.2017	05	Harmonization of thermal grease thicknesses (Table 18).	65
30.07.2021	06	General update of content Extended characterization of pin current carrying capability Removal of Mounting specifications	20

## Introduction

SEMITOP®Classic is an established platform introduced in the market in the late 90's. It is a products line available in four different housing sizes capable to cover a very wide range of applications, from Soft Starters up to Solar. Product is designed for all applications where performance, reliability, integration and costs are a must.

### SEMITOP®Classic key-features

- Single Screw for fast and reliable assembly process
- 12 mm height module compatible with SEMITOP®E1/E2
- No baseplate
- Press-fit and Solder terminals
- Four packages (1,2,3,4)
- Terminals on edges for simplified PCB routing
- Wide range of applications
  - ✓ Soft Starters
  - ✓ Welding
  - ✓ Switched Mode Power Supply
  - ✓ UPS
  - ✓ Solar



## 1. Technical details

### 1.1 Designation system

Table 1: Designation system							
<b>SK</b>	<b>50</b>	<b>GD</b>	<b>06</b>	<b>6</b>	<b>E</b>	<b>T</b>	<b>p</b>
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
<p><b>(1)</b> SK = SEMIKRON product</p> <p><b>(2)</b> Current rating [A] = approximate nominal current</p> <p><b>(3)</b> Topology (circuit description)</p> <ul style="list-style-type: none"> <li>➤ KQ = Single pair of Antiparallel Thyristors</li> <li>➤ WT = Double pair of Antiparallel Thyristors</li> <li>➤ UT = Triple pair of Antiparallel Thyristors</li> <li>➤ B = Single Phase Bridge Rectifier</li> <li>➤ D = 3-phase Bridge Rectifier</li> <li>➤ GAL = Single Boost – IGBT based (G)</li> <li>➤ DGL = 3-phase Bridge Rectifier + Chopper – IGBT based (G)</li> <li>➤ DGDL = CIB (3-phase rectifier + brake + 3-phase inverter) – IGBT based (G)</li> <li>➤ GD = Sixpack (3-phase inverter) – IGBT based (G)</li> <li>➤ GH = H-Bridge (1-phase Full-Bridge) – IGBT based (G)</li> <li>➤ MLI = 3-Level NPC (Multi Level Inverter)</li> <li>➤ TMLI = 3-Level T-NPC (T-type Multi Level Inverter)</li> </ul> <p><b>(4)</b> Voltage rating</p> <ul style="list-style-type: none"> <li>➤ Thyristor/diode: <math>V_{RRM}</math> [V]/100 <ul style="list-style-type: none"> <li>○ 16 for 1600V</li> <li>○ 12 for 1200V</li> <li>○ 08 for 800V</li> </ul> </li> <li>➤ IGBT: <math>V_{CE}</math>[V]/100 <ul style="list-style-type: none"> <li>○ 12 for 1200V</li> <li>○ 06 for 600V</li> <li>○ 07 for 650V</li> </ul> </li> <li>➤ MOSFET: <math>V_{DS}</math>[V]/10 <ul style="list-style-type: none"> <li>○ 120 for 1200V</li> <li>○ 10 for 100V</li> </ul> </li> </ul> <p><b>(5)</b> Optional: IGBT technology</p> <ul style="list-style-type: none"> <li>➤ 6 = Trench IGBT3</li> <li>➤ E3 = Trench IGBT3</li> <li>➤ F3 = Trench IGBT3 Fast</li> <li>➤ T4 = Trench4</li> <li>➤ F4 = Trench4 Fast</li> </ul> <p><b>(6)/(7)</b> Optional (can be used in combination):</p> <ul style="list-style-type: none"> <li>➤ T = Temperature sensor</li> <li>➤ E = Open Emitter</li> <li>➤ I = Current sensor</li> <li>➤ D1 = Rapid switching diode</li> <li>➤ SC = Silicon Carbide (typically representative of Schottky Diode)</li> </ul> <p><b>(8)</b> PCB contact technology</p> <ul style="list-style-type: none"> <li>➤ unspecified = Solder terminals</li> <li>➤ p = Press-Fit terminals</li> </ul>							

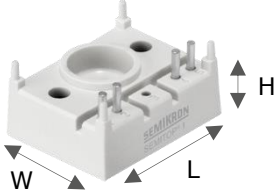



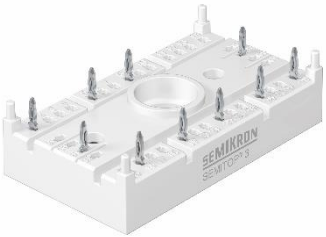
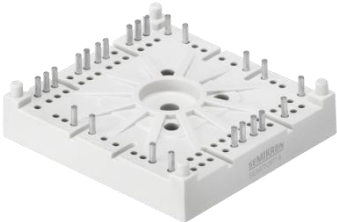

## 1.2 Tolerances system

SEMITOP®Classic have been designed according to tolerances defined by ISO 2768-m. The value of tolerance depends on the value of the nominal dimension, usually the greater is the nominal dimension the greater is the corresponding tolerance. Following the values of tolerance from ISO 2768-m, according to the different dimensional ranges, SEMITOP® E tolerances are:

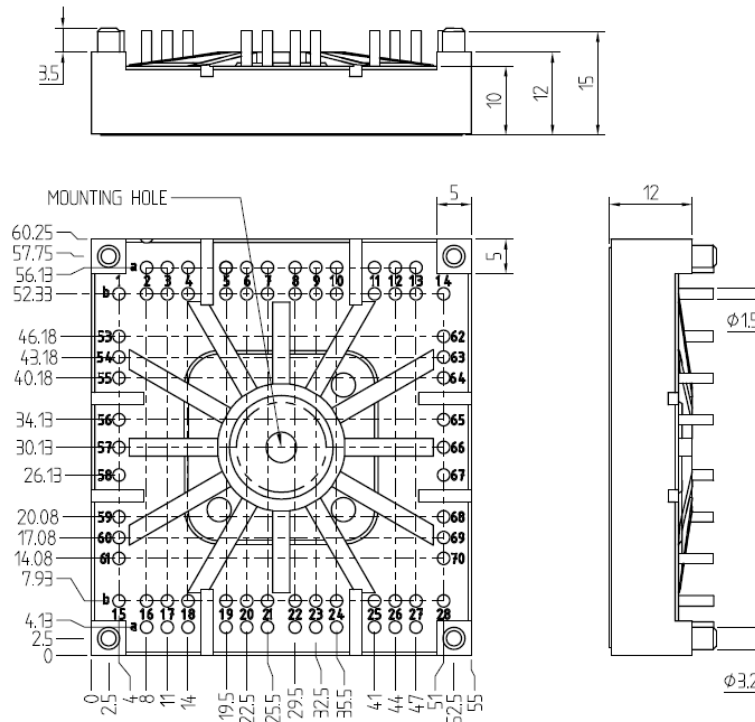
Table 2: Tolerances system [mm]	
$0.5 \leq x \leq 3$	$\pm 0.1$
$3.0 \leq x \leq 6$	$\pm 0.1$
$6 \leq x \leq 30$	$\pm 0.2$
$30 \leq x \leq 120$	$\pm 0.3$

Dimensions for all SEMITOP®Classic in the datasheets are according to the above mentioned tolerance system, unless otherwise specified.

Figure 1 and Figure 2 provide a comprehensive view of the SEMITOP®Classic outline.

Figure 1: SEMITOP®Classic housing size dimensions			
Housing	Solder	Press-Fit	Dimensions in mm (LxWxH)
SEMITOP®1		Not available	31 x 24 x 12
SEMITOP®2			40.5 x 28 x 12
SEMITOP®3			55 x 31 x 12
SEMITOP®4			60 x 55 x 12

**Figure 2: SEMITOP®4 Dimensions (Example)**



Dimensions in millimeters

### 1.3 Insulation properties

SEMITOP®Classic modules comply with the creepage and clearance distances required by DIN EN 50178, EN62477-1 and EN61800-5-1 by cases, with the following boundary conditions:

- Maximum mains voltage (line to line) 220V, 480V, 690V
- Maximum DC-link voltage (rms) 450V, 850V, 1250V
- Maximum peak voltage in circuit (rated chip voltage) 650V, 1200V, 1700V
- Line over-voltage category 3
- Pollution degree 2
- Maximum height of operation above sea level 3000 m
- Protective separation for T-sensors Functional insulation

### 1.4 Housing Material

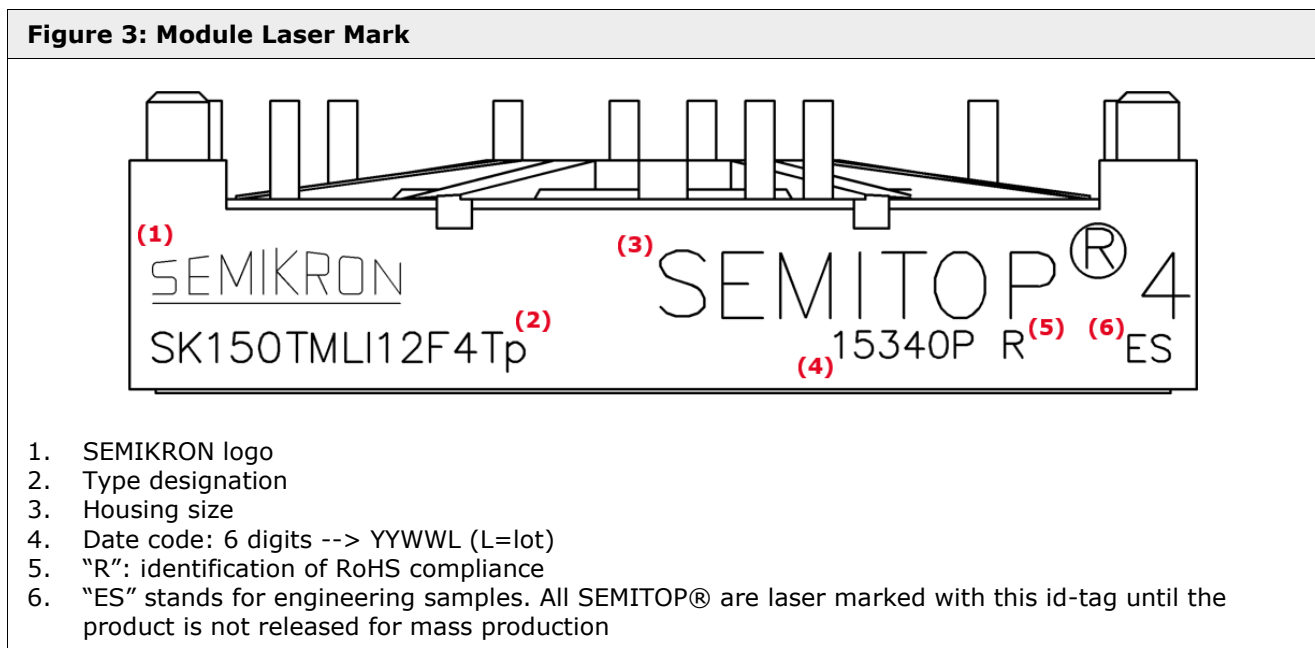
The SEMITOP®Classic housing material is an advanced fiberglass reinforced compound material that provides improved mechanical and electrical strength. This material is ready for latest chip generations and allows operation up to  $T_j=175\text{ °C}$ .

**Table 3: Housing properties**

	Min.	Typ.	Max.	Unit
Case temperature			125	°C
CTI	325			
RTI			140	°C

### 1.5 Laser marking

All SEMITOP®Classic modules are laser marked before shipment, according to the below picture:

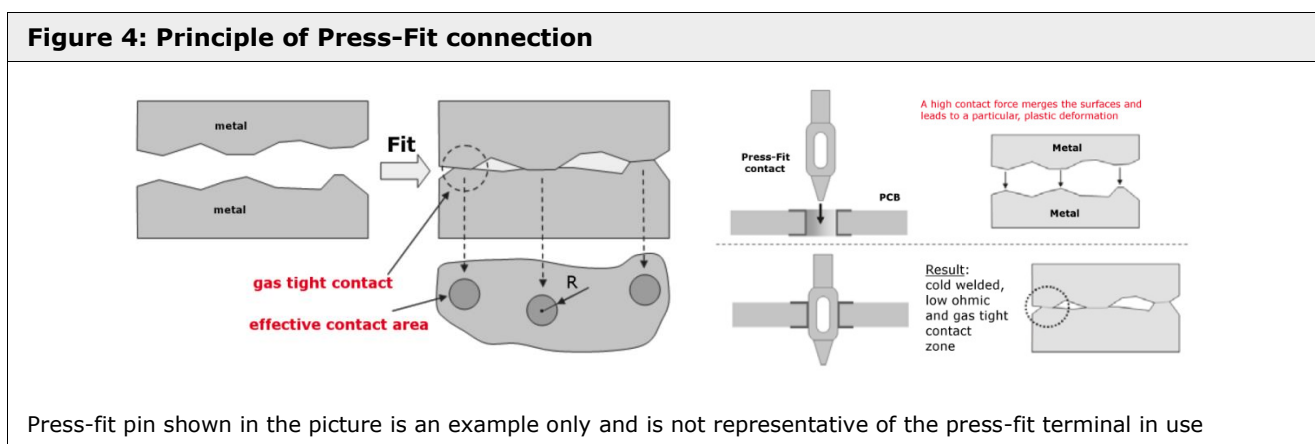


### 1.6 Press-fit pin

SEMITOP®Classic is available with Solder and Press-fit pins. While having similar a cost, the press-fit technology allows assembly of module onto PCB either by soldered or solder-free process.

Solder free joint to the PCB is based on the following physical phenomenon: if two contact faces of a connection are fitted together, there are only a few spots which are really connected (metal to metal) and which carry the current – also for polished surfaces. The minimum radius of such a microscopic metal-metal contact is typically 10µm. In force fitting technologies like Press-Fit, there is always a necessary plastic deformation on these really effective contact points within the contact zone, due to the high contact pressure that occurs since the macroscopic contact force concentrates on a small microscopic contact area. That means the two faces will be merged. Thus, the effective contact zone will be increased and, most importantly, a gas tight contact zone is generated, which is very robust against corrosive environments.

The connection principle is the well-known cold welding effect: free electrons are generated out of the plastic deformation of both contact faces. The metal-bond electron cloud links the free electrons and connect them again with the same mechanism as in the basic metal. The bonding force increased within the first hours of the connection due to recrystallizations effects.



Furthermore, mounting process is conducted at room temperature leading to additional benefits of no extra heating process for surface mounted devices and no need to use heat resistant plastics for the connector housing.

### 1.6.1 Mechanical details

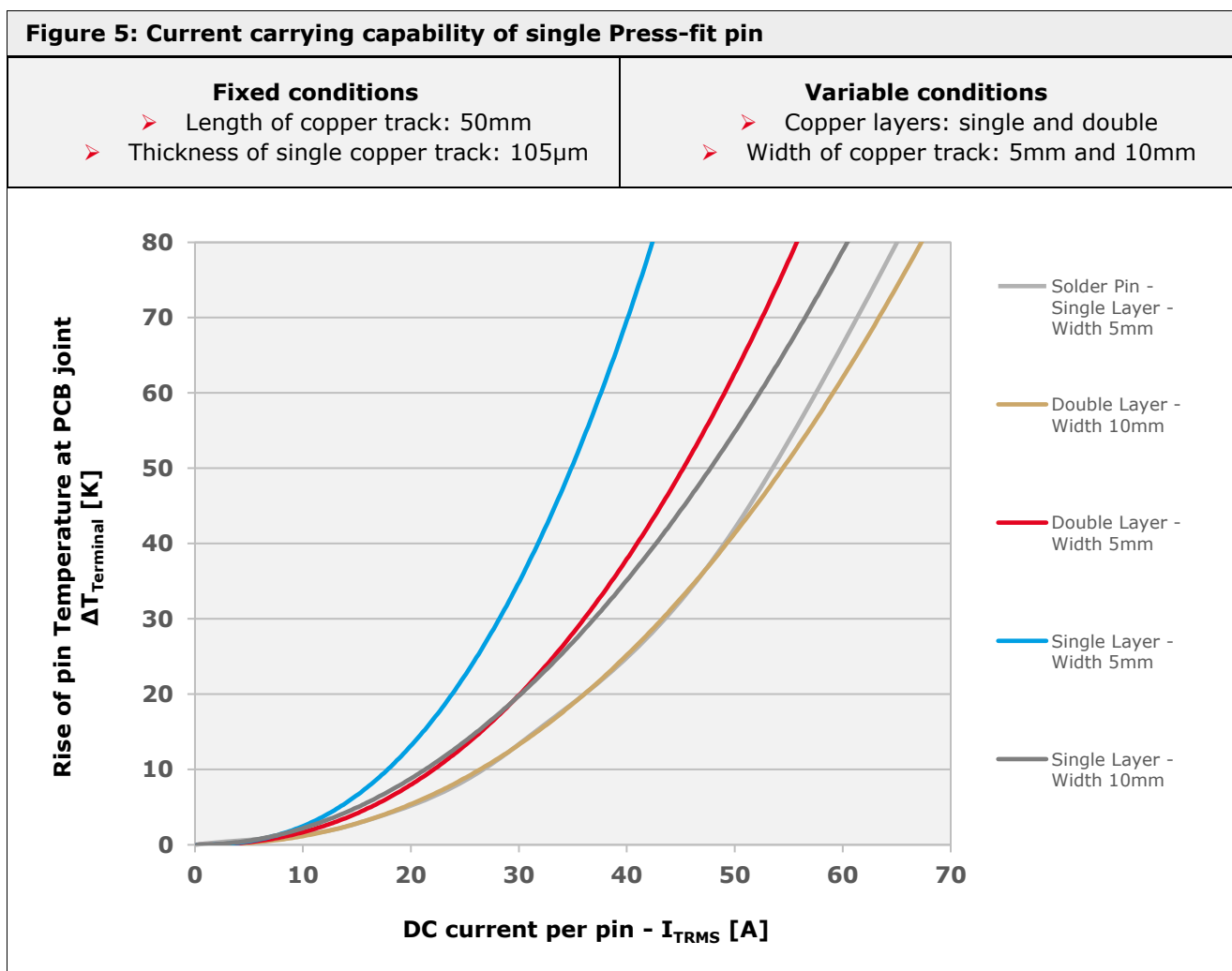
Key features of the pin are:

- Rounded tip to maintain integrity of via plating and allow reuse
- Mechanical stress relief at the pin base
- Compliancy with DIN and IEC standards

Further details are available upon request.

### 1.6.2 Current carrying capability

The pin current capability is strongly influenced by the boundary conditions of the specific application in use (i.e. PCB layout, heatsink temperature, ambient temperature and cooling conditions) and cannot be given as a simple value. Figure 5 shows how temperature at Pin-to-PCB joint ( $T_{\text{terminal}}$ ) increases when current is flowing through the single pin, under four different conditions of PCB layout. Current capability of Solder Pin is also shown as reference.



$\Delta T_{\text{terminal}} = T_{\text{terminal1}} - T_{\text{terminal0}}$ , where:

- $T_{\text{terminal0}}$  is starting temperature when no current flows through terminal. Value depends on several factors but is typically somewhere between  $T_{\text{amb}}$  and  $T_{\text{sink}}$ .
- $T_{\text{terminal1}}$  is steady state temperature when current flows through terminal. This is the factor limiting maximum current terminal can carry.

It can be observed that PCB design has a significant impact on the current carrying capability. For instance,  $I_{TRMS}$  value at same temperature rise can be almost doubled when moving from single layer 5mm to double layer 10mm copper track.

Above diagrams and considerations are valid when considering one single pin. In case of pins in parallel, particular attention must be paid to a derating factor which is introduced by thermal cross-talk between neighbor pins. As a general rule, the greater the distance between pins the lower the derating factor per each single pin. Nevertheless, for a fixed pin-to-pin distance, measurements revealed that such a derating factor is, again, strongly influenced by PCB features.

Test results show that, under following conditions:

- Length of copper track (distance between PCB-to-pin joint and current source): 50mm
- Thickness of single copper track (all over the track length): 105 $\mu$ m
- Copper layers: double layer
- Width of copper track (all over the track length): 10mm

when 2x neighbor pins system conduct 2x current of single pin system, resulting  $\Delta T_{Terminal}$  is higher than the one achieved in the single pin system. On the other way round, same  $\Delta T_{Terminal}$  can be achieved by both systems when each single pin of the 2x pins system conducts approximately 25% less current than the single pin system. Therefore, for a given  $\Delta T_{Terminal}$ , if  $I_{TRMS}^{(1pin)}$  is the current of a single pin system, current of the 2x pins system would be approximately  $I_{TRMS}^{(2pin)} = 2 \times 0.75 \times I_{TRMS}^{(1pin)}$ . Derating factor is intended to decrease with following factors:

- increase of the distance between pins (how fast depends on PCB features)
- increase of heat dissipation capability of the PCB. This can be achieved by increasing cross-section area of the copper track (Thickness and Width).

### 1.6.3 Further observations

As mentioned before, Press-fit pin can be either soldered or solder-free pressed into PCB. Adopted mounting process (solder or solder-free), determines the absolute maximum temperature limit that pin can reach in safe and reliable conditions. Nevertheless, in order to exploit benefits of the press-fit technology at best, press-fit pins and PCB have to be assembled by solder-free press-in process.

- **Soldered mounting process:** The main limiting factor related to the lifetime of the solder joint of the pin-to-PCB contact is the re-crystallization phenomenon of the solder alloy. For SAC 97.5%Sn-2%Ag-0.5%Cu solder alloys, in order to prevent from this phenomenon, it is recommended to keep operating temperature of the solder joint far below 110°C (recommended maximum operating  $T_{terminal} = 85^\circ\text{C}$ ). Different solder alloys may raise up the limit, though other physical limits of the surrounding components and PCB have to be considered.
- **Solder-free mounting process by press-in:** In this case, as mentioned above, the connection between pin and PCB is ensured by the cold welding phenomenon. Thus, the real limit of the formed joint it's not strictly related to the joint itself, because in the cold welding phenomenon a certain level of mechanical friction it is always present (which also explain the higher reliability of press-fit in harsh environments). The limit is indeed related to the glass transition temperature  $T_g$  of the PCB. For a standard FR4-02 PCB with  $T_g = 140^\circ\text{C}$ , a maximum operating temperature of 110°C is recommended. Consequently, a PCB with higher  $T_g$ , would lead to higher limit of temperature rise.

## 1.7 Specification of Integrated Temperature Sensor

All SEMITOP IGBT modules feature a temperature-dependent resistor for temperature measurement. It is important to remark that, although the resistor is soldered onto the DBC ceramic substrate along with chips, it does not reflect junction temperature but it can be considered as an indicator for the DBC and heatsink temperature. For details on how junction temperature can be estimated out of temperature measured by sensor, please refer to dedicated [Application Note AN 20-001](#) [2].

### 1.7.1 Electrical characteristics

The standard "KG3B" temperature sensor exhibits a negative temperature coefficient characteristic with a nominal resistance value at 25°C of 5k $\Omega$ ±5%. The temperature-dependent resistance of the NTC sensor is described by the following equation:

**Table 4: NTC general equation and main parameters**

$$R_2 = R_1 \cdot e^{[B(T_1/T_2) \cdot (\frac{1}{T_2} - \frac{1}{T_1})]}$$

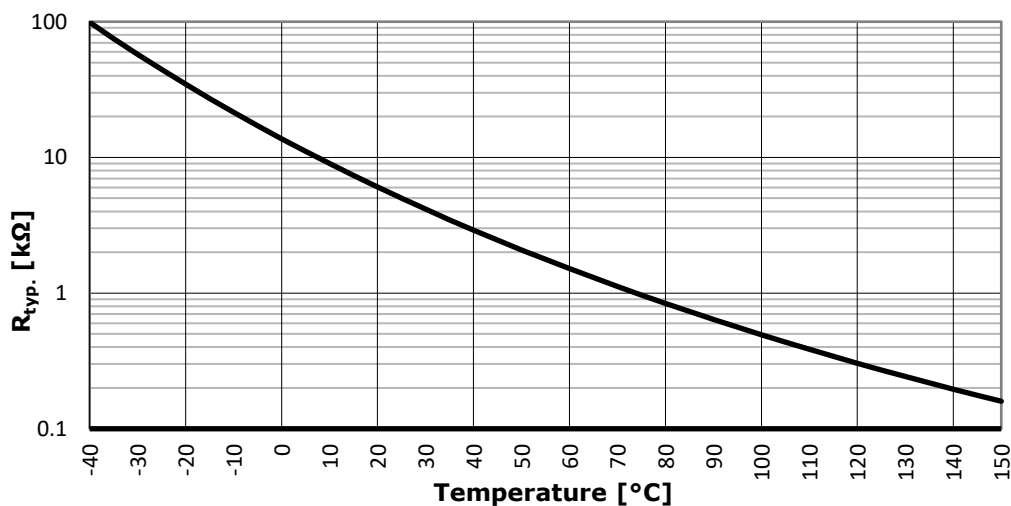
R<sub>2</sub> : resistance at absolute temperature T<sub>2</sub> [K]

R<sub>1</sub> : resistance at absolute temperature T<sub>1</sub> [K]

B : B-value B<sub>(T<sub>1</sub>/T<sub>2</sub>)</sub> [K]

Symbol	Tolerance	min	typ	max	Unit
R <sub>25</sub>	±5%	4.75	5.00	5.25	kΩ
R <sub>100</sub>	±5%	468	493	518	Ω
B <sub>(25/50)</sub>			3375		K
B <sub>(25/85)</sub>			3420		K
B <sub>(100/125)</sub>			3550		K

**Figure 6: Typical NTC characteristic**



### 1.7.2 Electrical insulation

Since the SEMITOP®Classic module is filled with silicone gel for insulation purposes, the requirements for the specified insulation voltage (AC/2.5kV/1 min, AC/3kV/1s at 50Hz) are met and 100% tested.

Nevertheless, insulation properties may be endangered when short circuit failure and/or electrical overstress occur. The reason is that, during such failure events, the bond wires on the chips could melt off and generates an arc with high energy plasma. In this case, the direction of plasma expansion is not predictable and the temperature sensor may be touched by plasma thus exposed to a high voltage.

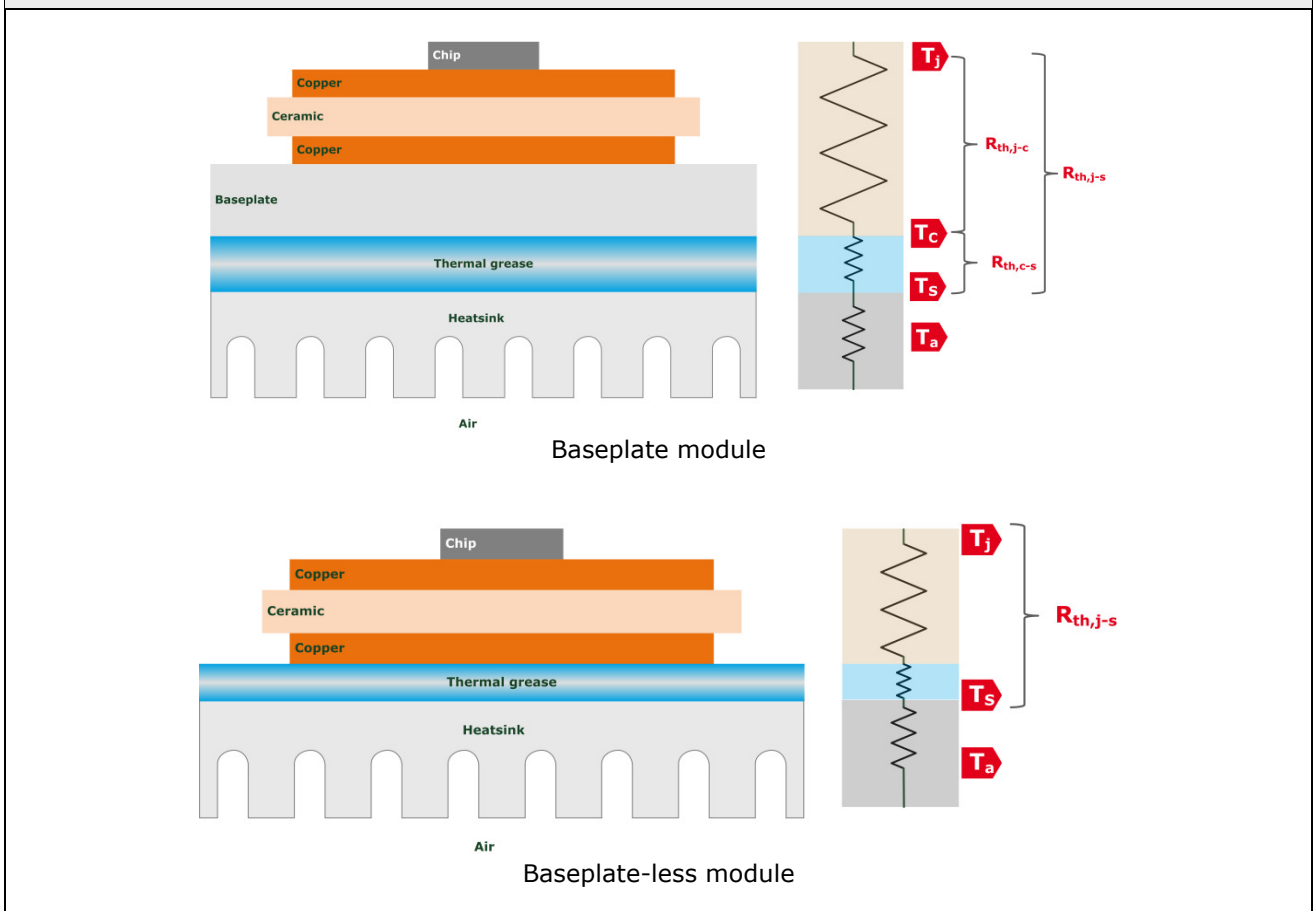
The safety grade "Safe electrical insulation" according to EN 50178 can be achieved by different additional means, described there in detail.

### 1.8 Thermal performance

SEMITOP®Classic are baseplate-free power modules where dice are placed on a DBC substrate. This DBC substrate is made of a top side copper layer in direct contact with the chip, a ceramic layer that ensures insulation and a back side copper layer that goes in contact with the heatsink through a thermal grease layer. Modules with baseplate technology feature the system DBC substrate + chips soldered to a copper baseplate. The whole assembly is then in contact with the heatsink through a thermal grease layer.

This technological difference brings to different thermal resistance paths as shown in the following picture:

**Figure 7: Thermal resistance paths for a baseplate and a baseplate-less module**



By using a baseplate free module technology, there is a direct thermal path between chip junction and heatsink ( $R_{th,j-s}$ ). A module with baseplate considers two thermal paths: junction-case ( $R_{th,j-c}$ ) and case-sink ( $R_{th,c-s}$ ). Therefore, maximum allowable DC current capability performance for a SEMITOP®Classic module are always referred to the heatsink temperature. Attention has to be paid when comparing SEMITOP®Classic against module with baseplate in order to avoid misleading evaluations.

As example, a 50A/3phase inverter application has been simulated comparing SEMITOP®Classic against some competitors:

**Table 5: IGBT performance comparison (different reference point)**

	Module height [mm]	Module technology	$I_c$ [A] at $T_{j,max}$ and $T_s=25^\circ C$	$I_c$ [A] at $T_{j,max}$ and $T_s=70^\circ C$	$I_c$ [A] at $T_{j,max}$ and $T_c=25^\circ C$	$R_{th,j-s}$ [K/W]	Typical $V_{CE,sat}$ [V] at $I_{C,nom}$ and $T_j=150^\circ C$
SEMITOP*	12	No baseplate	60	50 <sup>(1)</sup>		1,11	1,65
Competitor A*	12	No baseplate			70 <sup>(2)</sup>	1,46	1,70
Competitor B*	12	No baseplate		45 <sup>(3)</sup>		1,25	1,75

\*Source: Datasheet available in the web

(1): current capability is referred to the heatsink

(2): current capability is referred to the case temperature in the datasheet

(3): current capability is referred to heatsink but at 80°C

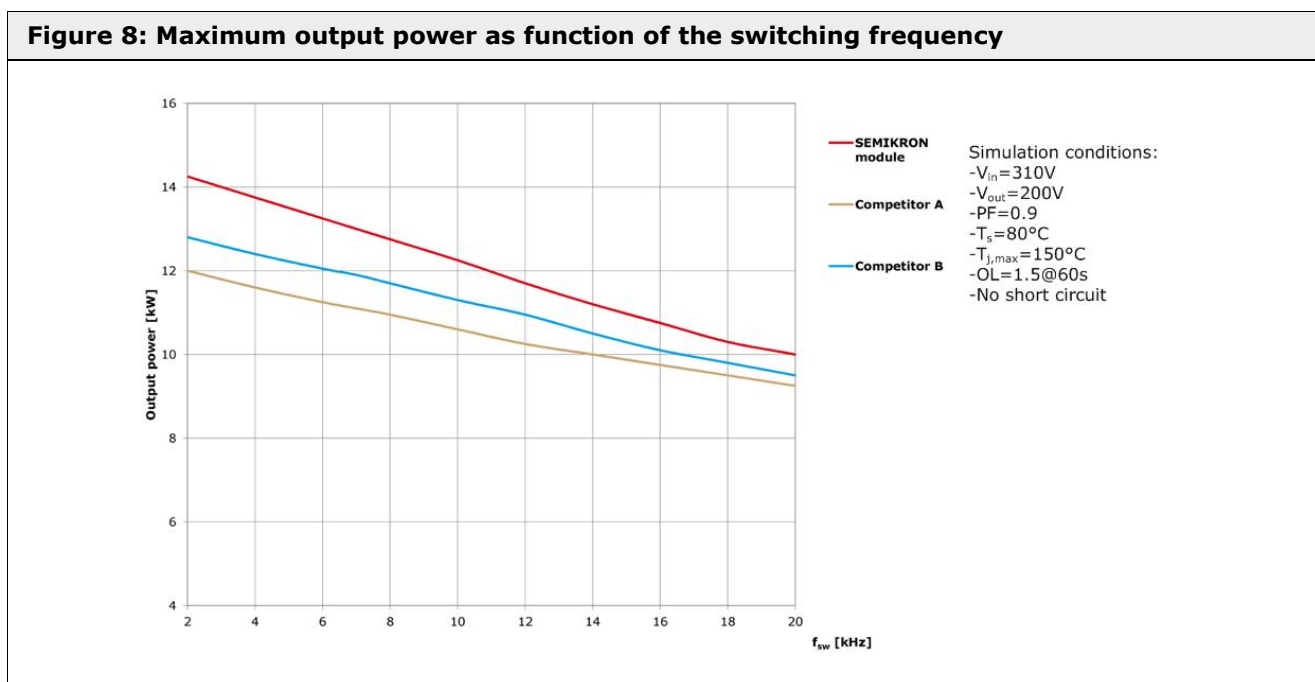
In order to make the right performance comparison, current capability should be calculated at the same reference point. By referring all the calculations to the same heatsink reference point, the IGBT performance are as per below table:

<b>Table 6: IGBT performance comparison (same reference point)</b>				
	<b>Module height [mm]</b>	<b>I<sub>c</sub> [A] at T<sub>j,max</sub> and T<sub>s</sub>=25°C</b>	<b>I<sub>c</sub> [A] at T<sub>j,max</sub> and T<sub>s</sub>=70°C</b>	<b>R<sub>th,j-s</sub> [K/W]</b>
SEMITOP*	12	60	50	1,11*
Competitor A*	12	50	40	1,46*
Competitor B*	12	54	44	1,25*

\*Source: Datasheet available in the web

SEMITOP®Classic exhibits the best thermal and electrical performance for the same reference point with the lowest R<sub>th,j-s</sub> value. The thermal resistance affects the maximum junction temperature and therefore the maximum output power as well as chip lifetime.

The picture shows the maximum output power vs switching frequency at the same switching conditions:



SEMITOP®Classic allows a 5-20% higher output power over a wide frequency range.

### 1.8.1 Properties and thickness of materials between chip and heatsink

Table 7 below gives a detailed cross-section overview of thicknesses and thermal properties of all the materials between chip and heatsink (TIM excluded). Information about some chips technologies are given as an example, details related to a specific product (chips, layout) can be provided upon request.

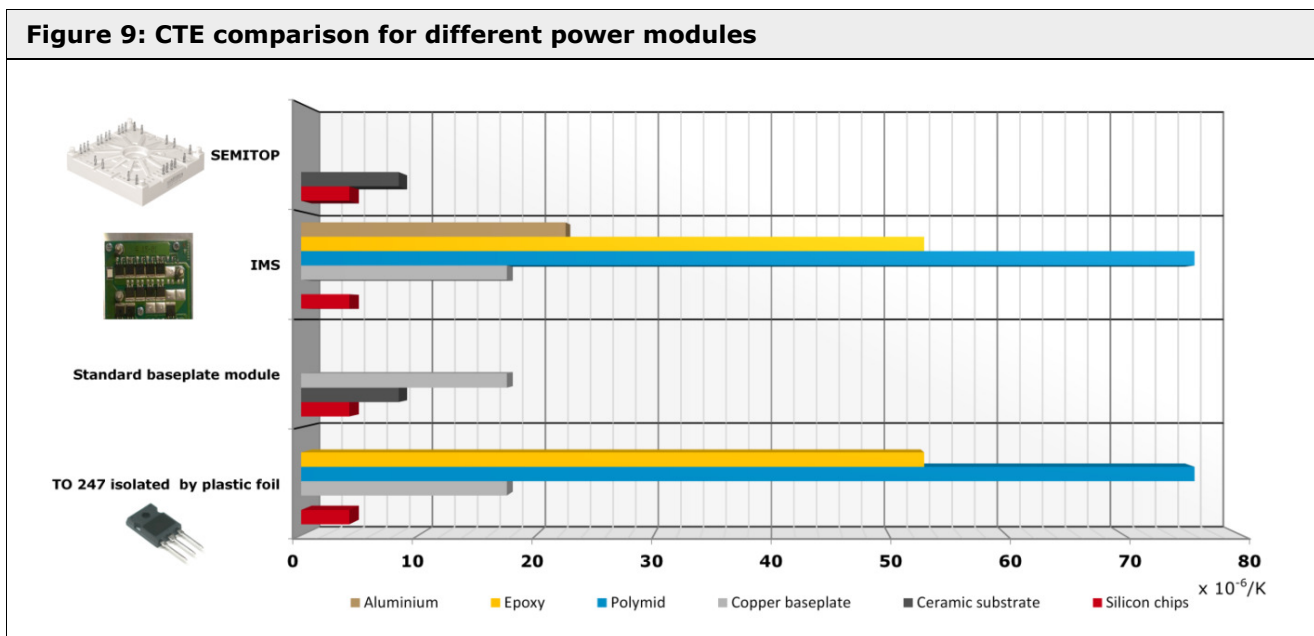
Layer	Material	Layer thickness [µm]	Spec. Thermal conductivity $\lambda$ @25°C [W/(m*K)]	Spec. Thermal Capacity @25°C [J/(kg*K)]	Density @25°C [kg/m³]
1200V IGBT T4	Si	115	148	700...750	2330
1200V CAL4F diode	Si	261	148	700...750	2330
1600V PEP Net diode	Si	310	148	700...750	2330
Chip solder layer	SnAg	~100	57	214	7800
DBC Copper (top)	Cu	300**	394	385	8960
DBC Ceramic	Al <sub>2</sub> O <sub>3</sub> *	630**	24	830	3780
DBC Copper (bottom)	Cu	300**	394	385	8960
Thermal Interface Material (TIM)	Customer specific				

\*) Alternative materials are also available and can be evaluated on project basis  
 \*\*) Valid for SEMITOP®1,2,3 Solder and Press-fit. SEMITOP®4 is 0.2/0.38/0.3 mm and SEMITOP®4 Press-Fit is 0.4/0.5/0.4.

The above table shows that a limited number of materials is used inside a SEMITOP®Classic package and how these materials feature similar CTE values.

The below picture compares SEMITOP®Classic materials and related CTEs with the ones used inside baseplate (modules or discrete solutions). The length of the bars indicate the CTE values; huge differences in length are an indication of considerable stress. Some main advantages become therefore evident:

- reduced thermo-mechanical stress. Big differences in the CTEs lead to mechanical stress causing ageing of connections when they are exposed to temperature changes
- reduced risk of delamination effects and field failures
- higher assembly reliability
- better thermal cycling performance



### 1.8.2 Contact between module and heatsink

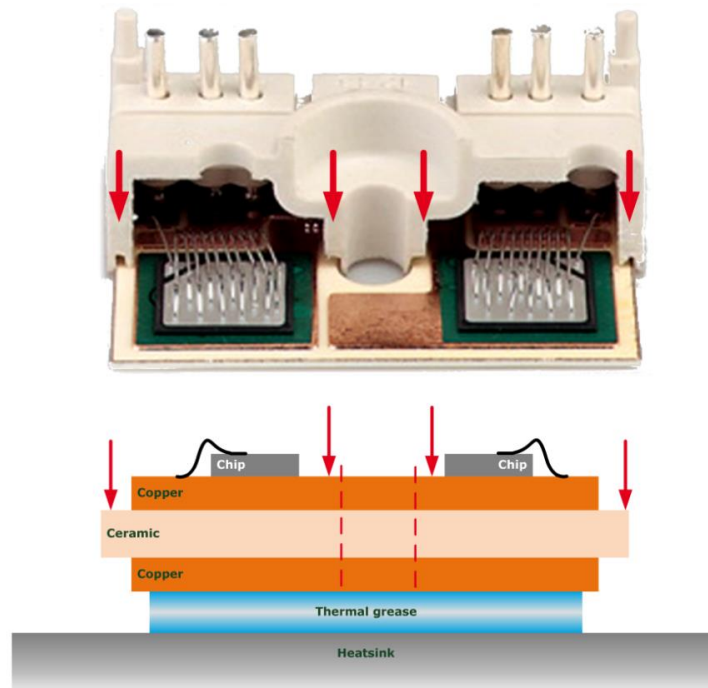
SEMITOP®Classic modules are made by direct soldering of the chips (IGBT, Mosfet, Diodes, Thyristors, SiC diodes and MOSFETs) and the power terminals on a ceramic substrate, typically Aluminium Oxide (Al<sub>2</sub>O<sub>3</sub>), covered by a thin copper layer.

The ceramic substrate is directly placed on the heatsink using a thermal conductive material (typically Thermal Grease) needed to fill all air gaps at the interface between the module and the heatsink.

The housing is the basic part of SKiiP® technology in SEMITOP®Classic modules: it has to guarantee that the ceramic substrate is evenly set on the heatsink in order to perform an homogenous heat exchange between module and the heatsink.

The SEMITOP® plastic housing has to evenly pressure the substrate surface through the only one required screw for the mounting.

**Figure 10: SEMITOP®Classic structure and concept of SKiiP technology**



The pressure concept brings the following advantages:

- Distributed pressure from the ceramic substrate (also called DBC) to heatsink without baseplate
- No stress on bonding connections
- No rigid large area connections between materials with different CTE (coefficient of thermal expansion)
- Different materials are contacted by a pressure system
- Any mechanical stress is absorbed by the structure itself

### 1.8.3 Definition and measurement of R<sub>th</sub>

The maximum junction temperature  $T_j$  under static and dynamic load conditions is very important for the power system layout, because it is a key factor for the lifetime of a power system.

The SEMITOP®Classic pressure contact technology thermally connects the DBC substrate to the heatsink; the case temperature  $T_c$  cannot be measured directly by a hole through the heatsink that allows the access to the module base. Therefore only the thermal resistance junction to heatsink  $R_{th,j-s}$  can be measured.

The thermal resistance  $R_{th,j-s}$  describes the distribution of temperatures in a system as the reaction to an impressed power  $P$  according to the following equation:

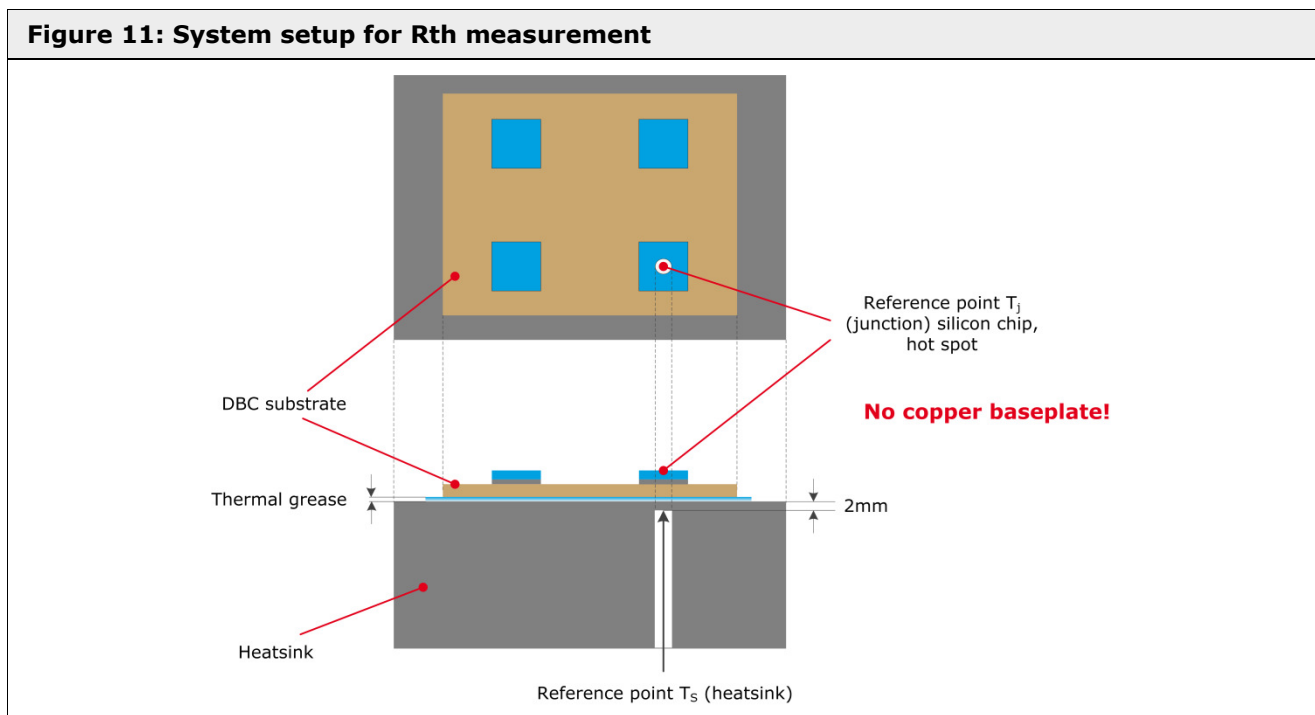
$$R_{th,j-s} = \frac{T_j - T_s}{P}$$

$T_j$  = junction temperature [°C]

$T_s$  = heatsink temperature [°C]

$P$  = impressed power [W]

The following picture shows the measure system for thermal resistance:



The reference point  $T_S$  is shifted to a position of 2mm underneath the module inside the heatsink. The distance of 2mm ensures that parasitic effects resulting from heatsink parameters (size, thermal conductivity etc.) are minimised and the disturbance induced by the thermocouple itself is negligible.

At position of hotspot, the heatsink will be drilled towards the bottom of the module to 2mm below the module DBC base (hole diameter of  $\varnothing$  2.5mm). A thermocouple can be introduced into this hole measuring the reference point  $T_S$ .

This method is independent from the DBC layout and results in constant thermal resistance values for the same chip sizes and packaging technology.

For modules without a baseplate it is not possible to measure the thermal resistance  $R_{th,j-c}$  and  $R_{th,c-s}$  separately as the baseplate does not exist. The thermal resistance  $R_{th,j-s}$  is evaluated from the virtual junction temperature  $T_j$ .

The following physical coherency is used: when operating with a small measurement current, bipolar semiconductor devices show a linear dependence of the voltage drop from the virtual junction temperature. The module is operated at a constant load current until thermal equilibrium is reached after 60 seconds. After reaching thermal equilibrium, the load current is switched off and a small current of 100mA is applied to the module.

### 1.9 Thermal Interface Materials (TIM)

All SEMITOP®Classic modules are available with pre-applied TIM:

- WP12 (Wacker-Chemie P12)
- HPTP (High Performance Thermal Paste)

Further information about TIM and Mounting Instruction can be found on website:

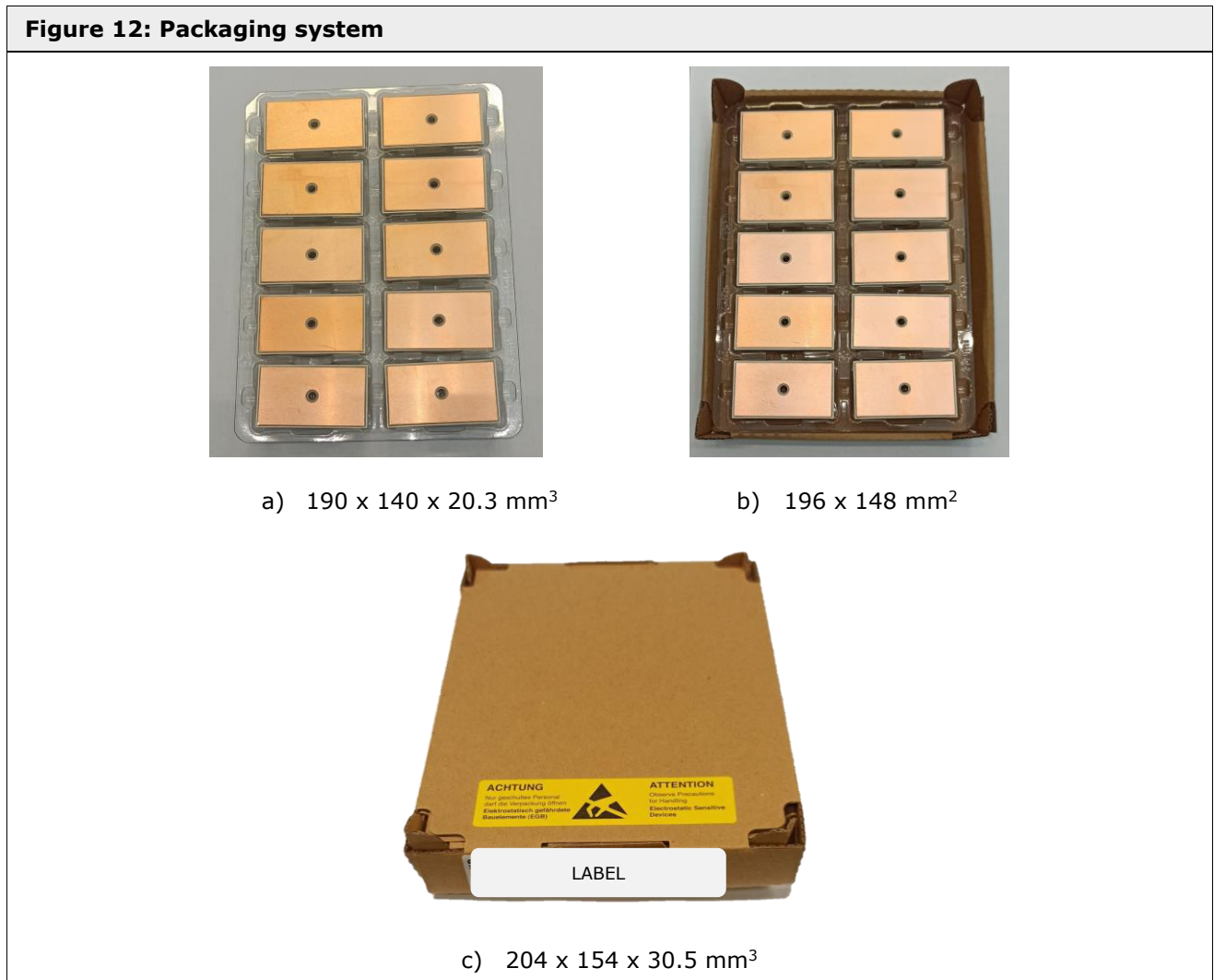
- [Technical explanation of TIM](#) [3]
- [General guidelines on TIM application](#) [4]
- [Mounting Instructions of SEMITOP®Classic](#) [5]

The typical  $R_{th(j-s)}$  values, shown in the SEMITOP®Classic datasheets, are valid for modules assembled onto the heatsink according to Mounting Instructions of SEMITOP®Classic and WP12 (0.8 W/(mK)).

## 2. Packaging specification

### 2.1 Packaging

SEMITOP®Classic modules are packed into ESD (not electrically chargeable) blisters (Figure 12a) and stored in a standard paper box (Figure 12b and 12c). Dimensions of paper box is the same for all SEMITOP®Classic.



Quantities per package depend on module size as per following table:

<b>Table 8: Number of modules per package</b>	
SEMITOP®1	<b>16x</b> modules/box
SEMITOP®2	<b>15x</b> modules/box
SEMITOP®3	<b>10x</b> modules/box
SEMITOP®4	<b>6x</b> modules/box

Two labels can be found on paper box (Figure 10c):

- **Yellow label:** warning for electrostatic sensitive devices.
- **White label:** information about product. Details about label content can be found here:
  - [Labeling of SEMIKRON product packaging](#)

Products with pre-applied TIM have additional labelling. Details can be found on website:

- [Technical Explanation of TIM \[3\]](#)

## 2.2 Storage and shelf life conditions

SEMITOP®Classic products are qualified according to IEC 60721-4-1 and can be stored in original package under following storage conditions:

<b>Table 9: Storage conditions</b>	
Duration	2 years
Climatic class	1K2 (IEC 60721-3-1)

Following shelf life conditions, which are not tested but based on SEMIKRON experience, are possible and should not be exceeded:

<b>Table 10: Shelf life conditions</b>	
Relative humidity	Max. 85%
Storage temperature	-25°C ... +60°C
Condensation	Not allowed at any time
Storage time	Max. 2 years

Different shelf life conditions may apply for modules with pre-applied TIM. Details can be found on website:

- [Technical Explanation of TIM \[3\]](#)

### 3. Reliability

#### 3.1 Qualification tests

The following tests are minimum requirements for the product release. Tests are being executed for release and re-qualification of new and/or re-developed modules. The scope of testing might be extended by further product-specific reliability tests.

Table 11: Qualification program	
Test Description	Conditions
<b>High Temperature Reverse Bias (HTRB)</b> IEC 60747-9:2007	1000h
	95% $V_{CE\ max}$
	$T_{j\ max}$
<b>High Temperature Reverse Bias (HTRB) *</b> IEC 60747-2:2016	1000h
	66% $V_{RRM}$
	$T_s = T_{j\ max} - 20K$
<b>High Temperature Gate Stress (HTGS)</b> IEC 60747-9:2007	1000h
	$\pm V_{GES\ max}$
	$T_{j\ max}$
<b>High Humidity High Temperature Reverse Bias (H3TRB)</b> EN 60749-5:2018, EN 60068-2-67:1996	1000h
	$T_a = 85^\circ C, RH = 85\%$
	$V_{CE} = \max. 80V$
<b>High Temperature Storage (HTS)</b> EN 60068-2-2:2008, IEC 60749-6:2002	1000h
	$T_{stg\ max}$
<b>Low Temperature Storage (LTS)</b> EN 60068-2-1:1993 + A1:1993 + A2:1994	1000h
	$T_{stg\ min}$
<b>Thermal Cycling (TC)</b> EN 60068-2-14:2010	100 cycles
	$T_{stg\ max} - T_{stg\ min}$
<b>Vibration</b> IEC 60068-2-6:2008	20Hz ... 500Hz Sinusoidal sweep
	5g
	2h per axis (x, y, z)
<b>Mechanical Shock</b> IEC 60068-2-27:2010	Half sine pulse 18ms
	30g
	3 times each direction ( $\pm x, \pm y, \pm z$ )
<b>Power Cycling (PC)</b> EN 60749-34:2010	>70k cycles at $\Delta T = 70K$

\*) Valid for standard glass passivated rectifier diodes and thyristors.

SEMİTOP® Classic modules can be subjected, on demand, to additional tests, as follows:

- Salt Spray Test according mil-std-810F method 509.4 +JESD22-a107-a
- Corrosive Atmosphere test according to DIN EN 60068-2-60Ke method 3 including  $SO_2$  in addition to  $H_2S$ ,  $NO_2$  and  $Cl_2$ .

Test level may vary, depending on module layout and technology

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### Symbols and Terms

A detailed explanation of the terms and symbols can be found in the "[Application Manual Power Semiconductors](#)" [6].

### References

- [1] [www.SEMIKRON.com](http://www.SEMIKRON.com)
- [2] [Calculating Junction Temperature using a Module Temperature Sensor \(AN\\_20-001 / 2020-01-29 – Rev-02\)](#)
- [3] [Thermal Interface Materials \(2019-09-25 - Rev-03\)](#)
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- [5] [Mounting Instruction SEMITOP®Classic \(2021-07-30 – Rev04\)](#)
- [6] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "[Application Manual Power Semiconductors](#)", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3

## **IMPORTANT INFORMATION AND WARNINGS**

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