Technical Explanation
SEMITOP® E1/E2

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Revision History

SEMIKRON reserves the right to make changes without further notice herein

Date	Revision n°	Description	Pages
25.03.2021	00	First release	18/18

Introduction

Exceeding the standard

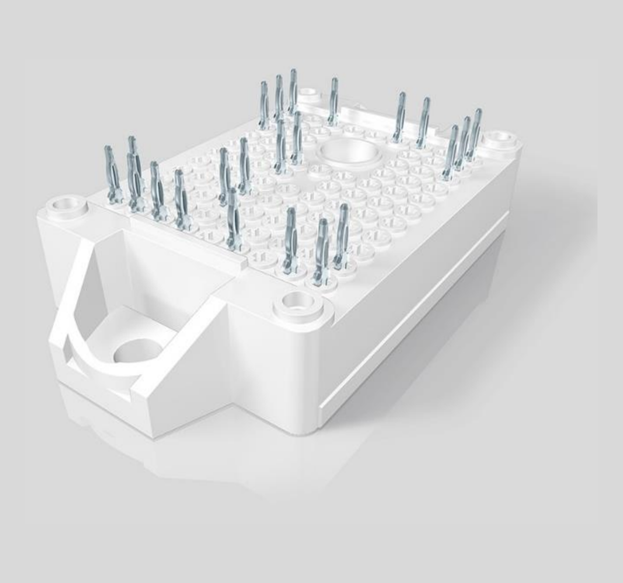
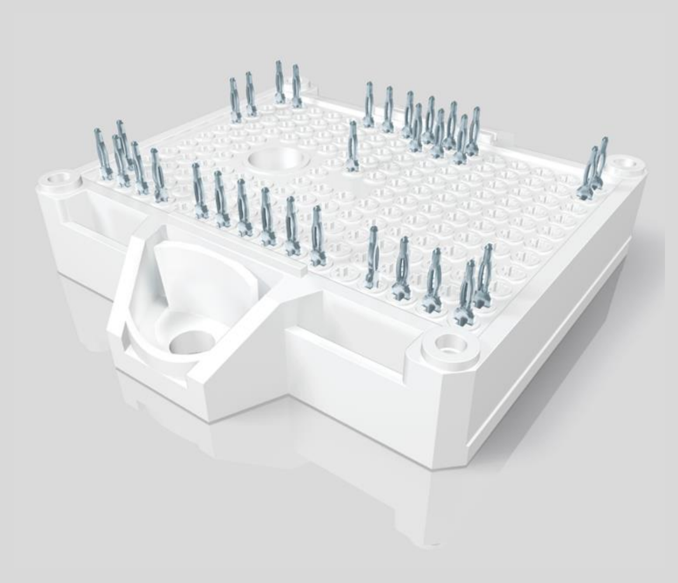
SEMITOP® 2nd generation (SEMITOP® E1/E2) fulfils the SEMIKRON target to offer a safe supply chain to the customers. The new packages represent the SEMITOP platform's natural evolution at enhanced performance levels, set to offer the best footprint, an extremely flexible architecture and high performing solutions at optimised system cost.

The latest Si and SiC chip technologies can be integrated to offer a competitive platform. Thus able to address the power modules demanding environment where high performance, innovation, quality standards and cost are the key winning factors. Thanks to a comprehensive portfolio with a large variety of configurations, SEMITOP®E1/E2 can address different markets like UPS, Solar, Motor Drives, Power Supplies, Energy Storage Systems, Welding and the new emerging EV battery charger market.

Developed as an extension of SEMITOP® 1st generation line up, SEMITOP® E pushes flexibility and power density to the limit, enabling platform to cover applications up to 200kW. SEMITOP® E is available in two different housing sizes, E1 and E2. Full compatibility with the existing standard industrial packages is ensured.

SEMITOP® E - key-features

- 12 mm height module compatible with SEMITOP® 1st generation (1,2,3,4)
- No baseplate
- Press-fit and Solder terminals
- Double screw for increased power density
- Thin ceramic and optimized pressure system to achieve best-in-class thermal performance for reduced operating temperatures and increased lifetime
- High performance plastic housing material with CTI 600
- Extreme flexibility on PCB-module interface, thanks to terminals matrix, enabling:
  - ✓ integration of complex topologies
  - ✓ extended range of customization
  - ✓ extremely low inductive design
  - ✓ integration of latest chip technology like SiC
- Wide range of applications up to 200kW
- Commodity product for supply chain safety

SEMITOP®E1	**SEMITOP®E2**
	

1. Technical details

1.1 Designation system

Table 1: Designation system

SK	25	DGDL	12	T7	E	T	E2	s
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)

(1) SK = SEMIKRON product

(2) Current rating [A] = approximate nominal current

(3) Topology (circuit description)
- DGDL = CIB (3-phase rectifier + brake + 3-phase inverter) – IGBT based (G)
- GD = Sixpack (3-phase inverter) – IGBT based (G)
- GH = H-Bridge (1-phase Full-Bridge) – IGBT based (G)
- MB = Half-Bridge (single leg of inverter) - MOSFET based (M)
- MLI = 3-Level NPC (Multi Level Inverter)
- AMLI = 3-Level Active NPC (Active Multi Level Inverter)
- TMLI = 3-Level T-NPC (T-type Multi Level Inverter)

(4) Voltage rating
- IGBT: V_{CE}[V]/100
    - 12 for 1200V
    - 06 for 600V
    - 07 for 650V
    - 10 for 950V
- MOSFET: V_{DS}[V]/10
    - 120 for 1200V

(5) Optional: IGBT technology
- 6 = Trench IGBT3
- E3 = Trench IGBT3
- F3 = Trench IGBT3 Fast
- T4 = Trench4
- F4 = Trench4 Fast
- L5 = Trench5 Low $V_{CE(sat)}$
- S5 = Trench5 High Speed Soft Switching
- H5 = Trench5 High Speed
- T7 = Generation 7 IGBT Low-Power
- L7 = Generation 7 IGBT Low $V_{CE(sat)}$
- CR03 = Planar Gen3 SiC Mosfet

(6)/(7) Optional (can be used in combination):
- T = Temperature sensor
- E = Open Emitter
- I = Current sensor
- D1 = Rapid switching diode
- SC = Silicon Carbide (typically representative of Schottky Diode)

(8) Ex (x=1, 2): Package
- SEMITOP E1
- SEMITOP E2

(9) PCB contact technology
- s = Solder terminals
- unspecified = Press-Fit terminals

1.2 Tolerances system

SEMITOP®E1/E2 have been designed according to tolerances defined by ISO 2768-m. The value of tolerance depends on the value of the nominal dimension, usually the greater is the nominal dimension the greater is the corresponding tolerance. Following the values of tolerance from ISO 2768-m, according to the different dimensional ranges, SEMITOP® E tolerances are:

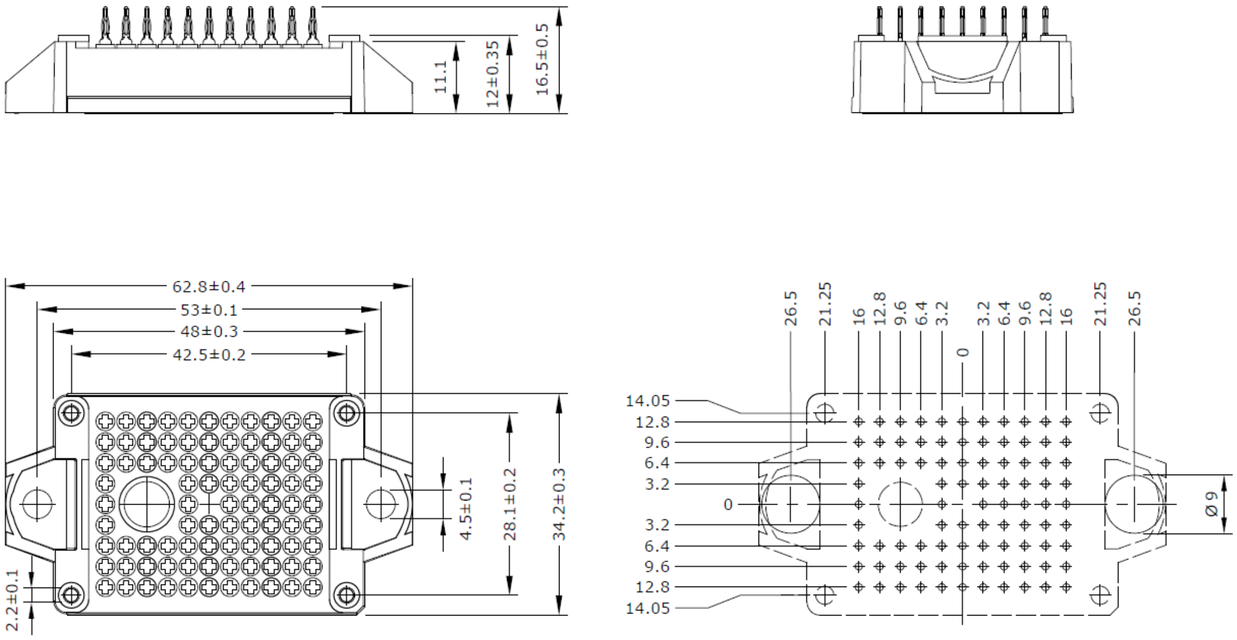
Table 2: Tolerances system [mm]

0.5 ≤ x ≤ 3	±0.1
3.0 ≤ x ≤ 6	±0.1
6 ≤ x ≤ 30	±0.2
30 ≤ x ≤ 120	±0.3

Dimensions for all SEMITOP® E1/E2 in the datasheets are according to the above mentioned tolerance system, unless otherwise specified.

Figure 1 and Figure 2 provide a comprehensive view of the dimensions of SEMITOP®E1 and SEMITOP®E2.

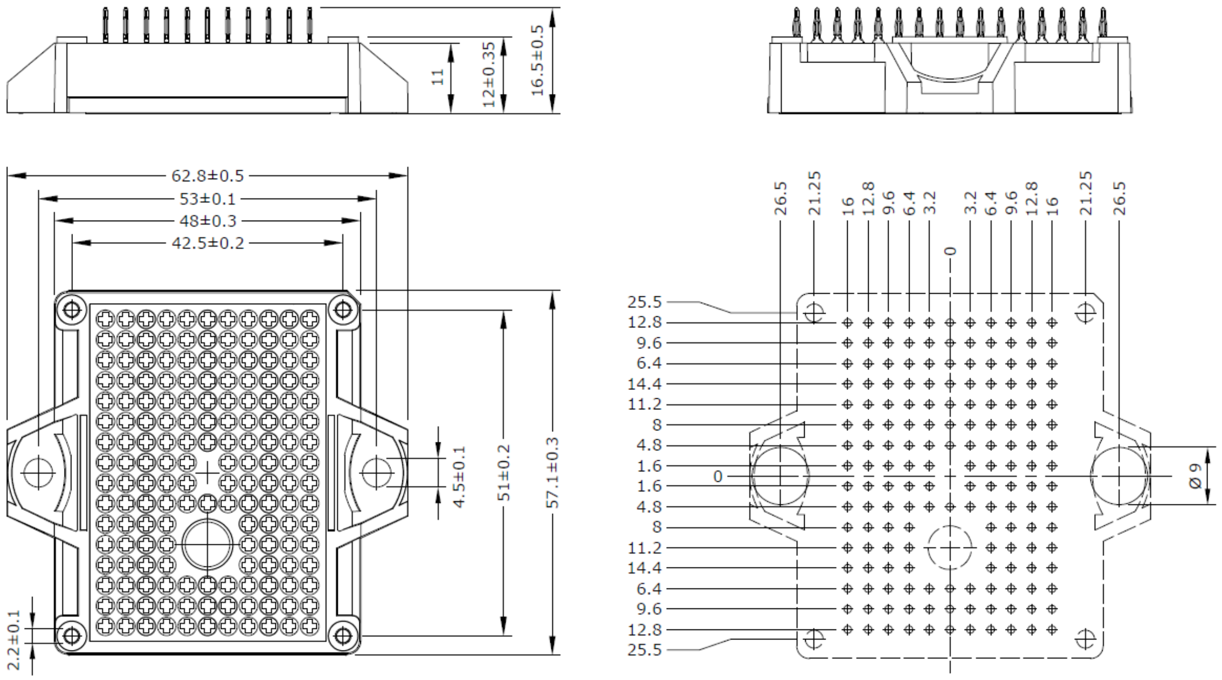
Figure 1: SEMITOP®E1 Dimensions



Dimensions in millimeters

Same housing for solder and press-fit terminals is used

Figure 2: SEMITOP®E2 Dimensions



Dimensions are in millimeters

Same housing for solder and press-fit terminals is used

1.3 Insulation properties

SEMITOP®E1/E2 modules comply with the creepage and clearance distances required by DIN EN 50178, EN62477-1 and EN61800-5-1 by cases, with the following boundary conditions:

➢ Maximum mains voltage (line to line)	220V, 480V, 690V
➢ Maximum DC-link voltage (rms)	450V, 850V, 1250V
➢ Maximum peak voltage in circuit (rated chip voltage)	650V, 1200V, 1700V
➢ Line over-voltage category	3
➢ Pollution degree	2
➢ Maximum height of operation above sea level	3000 m
➢ Protective separation for T-sensors	Functional insulation

1.4 Housing Material

The SEMITOP® E1/E2 housing material is an advanced fiberglass reinforced compound material that provides improved mechanical and electrical strength. This material is ready for latest chip generations and allows operation up to Tj=175 °C.

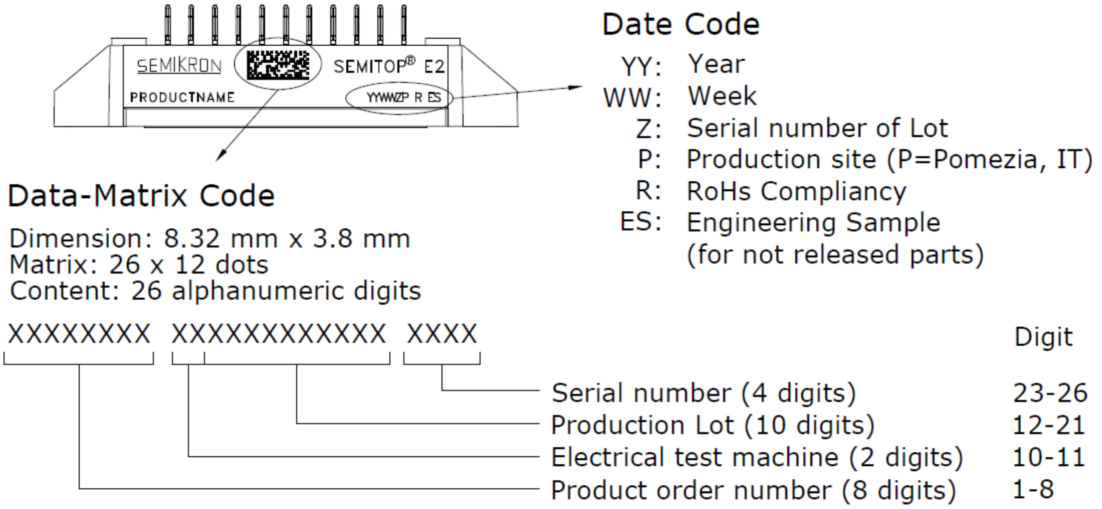
Table 3: Housing properties

	Min.	Typ.	Max.	Unit
Case temperature			125	°C
CTI	600			
RTI			140	°C

1.5 Laser marking

All SEMITOP®E1/E2 modules are laser marked before shipment, according to the below picture:

Figure 3: Module Laser Mark



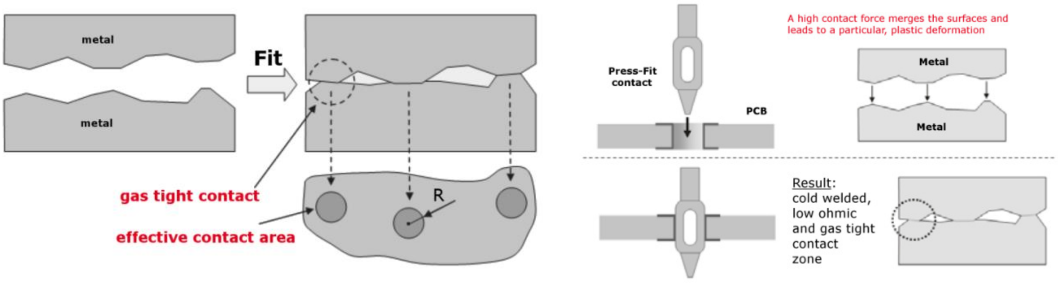
1.6 Press-fit pin

SEMITOP®E is available with Solder and Press-fit pins. While having similar a cost, the press-fit technology allows assembly of module onto PCB either by soldered or solder-free process.

Solder free joint to the PCB is based on the following physical phenomenon: if two contact faces of a connection are fitted together, there are only a few spots which are really connected (metal to metal) and which carry the current – also for polished surfaces. The minimum radius of such a microscopic metal-metal contact is typically 10µm. In force fitting technologies like Press-Fit, there is always a necessary plastic deformation on these really effective contact points within the contact zone, due to the high contact pressure that occurs since the macroscopic contact force concentrates on a small microscopic contact area. That means the two faces will be merged. Thus, the effective contact zone will be increased and, most importantly, a gas tight contact zone is generated, which is very robust against corrosive environments.

The connection principle is the well-known cold welding effect: free electrons are generated out of the plastic deformation of both contact faces. The metal-bond electron cloud links the free electrons and connect them again with the same mechanism as in the basic metal. The bonding force increased within the first hours of the connection due to recrystallizations effects.

Figure 4: Principle of Press-Fit connection



Press-fit pin shown in the picture is an example only and is not representative of the press-fit terminal in use

Furthermore, mounting process is conducted at room temperature leading to additional benefits of no extra heating process for surface mounted devices and no need to use heat resistant plastics for the connector housing.

1.6.1 Mechanical details

Key features of the pin are:

- Rounded tip to maintain integrity of via plating and allow reuse
- Mechanical stress relief at the pin base
- Compliancy with DIN and IEC standards

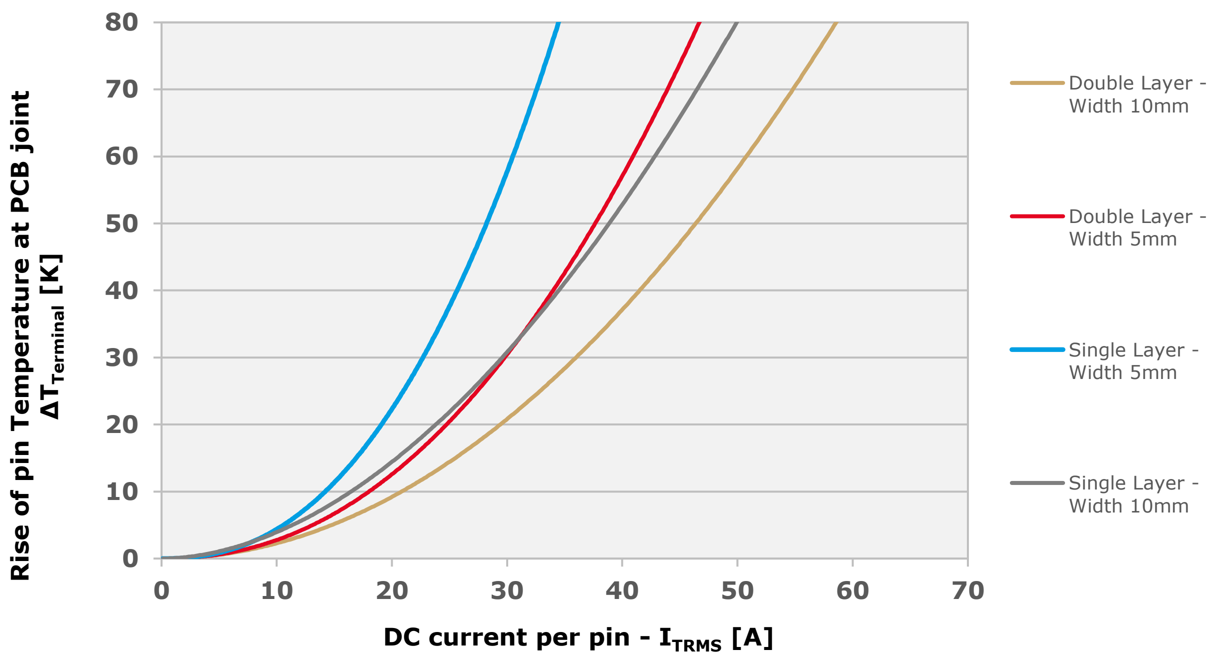
Further details are available upon request.

1.6.2 Current carrying capability

The pin current capability is strongly influenced by the boundary conditions of the specific application in use (i.e. PCB layout, heatsink temperature, ambient temperature and cooling conditions) and cannot be given as a simple value. Figure 5 shows how temperature at Pin-to-PCB joint ($T_{terminal}$) increases when current is flowing through the single pin, under four different conditions of PCB layout.

Figure 5: Current carrying capability of single Press-fit pin

Fixed conditions	**Variable conditions**
➢ Length of copper track: 50mm ➢ Thickness of single copper track: 105µm	➢ Copper layers: single and double ➢ Width of copper track: 5mm and 10mm



$\Delta T_{terminal} = T_{terminal1} - T_{terminal0}$, where:

- $T_{terminal0}$ is starting temperature when no current flows through terminal. Value depends on several factors but is typically somewhere between T_{amb} and T_{sink}.
- $T_{terminal1}$ is steady state temperature when current flows through terminal. This is the factor limiting maximum current terminal can carry.

It can be observed that PCB design has a significant impact on the current carrying capability. For instance, I_{TRMS} value at same temperature rise can be almost doubled when moving from single layer 5mm to double layer 10mm copper track.

Above diagrams and considerations are valid when considering one single pin. In case of pins in parallel, particular attention must be paid to a derating factor which is introduced by thermal cross-talk between neighbor pins. As a general rule, the greater the distance between pins the lower the derating factor per each single pin. Nevertheless, for a fixed pin-to-pin distance, measurements revealed that such a derating factor is, again, strongly influenced by PCB features.

Test results show that, under following conditions:

- Length of copper track (distance between PCB-to-pin joint and current source): 50mm
- Thickness of single copper track (all over the track length): 105µm
- Copper layers: double layer
- Width of copper track (all over the track length): 10mm

when 2x neighbor pins system conduct 2x current of single pin system, resulting $\Delta T_{Terminal}$ is higher than the one achieved in the single pin system. On the other way round, same $\Delta T_{Terminal}$ can be achieved by both systems when each single pin of the 2x pins system conducts approximately 25% less current than the single pin system. Therefore, for a given $\Delta T_{Terminal}$, if $I_{TRMS}^{(1pin)}$ is the current of a single pin system, current of the 2x pins system would be approximately $I_{TRMS}^{(2pin)}=2 \times 0.75 \times I_{TRMS}^{(1pin)}$. Derating factor is intended to decrease with following factors:

- increase of the distance between pins (how fast depends on PCB features)
- increase of heat dissipation capability of the PCB. This can be achieved by increasing cross-section area of the copper track (Thickness and Width).

1.6.3 Further observations

As mentioned before, Press-fit pin can be either soldered or solder-free pressed into PCB. Adopted mounting process (solder or solder-free), determines the absolute maximum temperature limit that pin can reach in safe and reliable conditions. Nevertheless, in order to exploit benefits of the press-fit technology at best, press-fit pins and PCB have to be assembled by solder-free press-in process.

- **Soldered mounting process:** The main limiting factor related to the lifetime of the solder joint of the pin-to-PCB contact is the re-crystallization phenomenon of the solder alloy. For SAC 97.5%Sn-2%Ag-0.5%Cu solder alloys, in order to prevent from this phenomenon, it is recommended to keep operating temperature of the solder joint far below 110°C (recommended maximum operating $T_{terminal}$=85°C). Different solder alloys may raise up the limit, though other physical limits of the surrounding components and PCB have to be considered.

- **Solder-free mounting process by press-in:** In this case, as mentioned above, the connection between pin and PCB is ensured by the cold welding phenomenon. Thus, the real limit of the formed joint it's not strictly related to the joint itself, because in the cold welding phenomenon a certain level of mechanical friction it is always present (which also explain the higher reliability of press-fit in harsh environments). The limit is indeed related to the glass transition temperature T_g of the PCB. For a standard FR4-02 PCB with T_g = 140°C, a maximum operating temperature of 110°C is recommended. Consequently, a PCB with higher T_g , would lead to higher limit of temperature rise.

1.7 Specification of Integrated Temperature Sensor

All SEMITOP IGBT modules feature a temperature-dependent resistor for temperature measurement. It is important to remark that, although the resistor is soldered onto the DBC ceramic substrate along with chips, it does not reflect junction temperature but it can be considered as an indicator for the DBC and heatsink temperature. For details on how junction temperature can be estimated out of temperature measured by sensor, please refer to dedicated Application Note AN 20-001.

1.7.1 Electrical characteristics

The standard "KG3B" temperature sensor exhibits a negative temperature coefficient characteristic with a nominal resistance value at 25°C of 5kΩ±5%. The temperature-dependent resistance of the NTC sensor is described by the following equation:

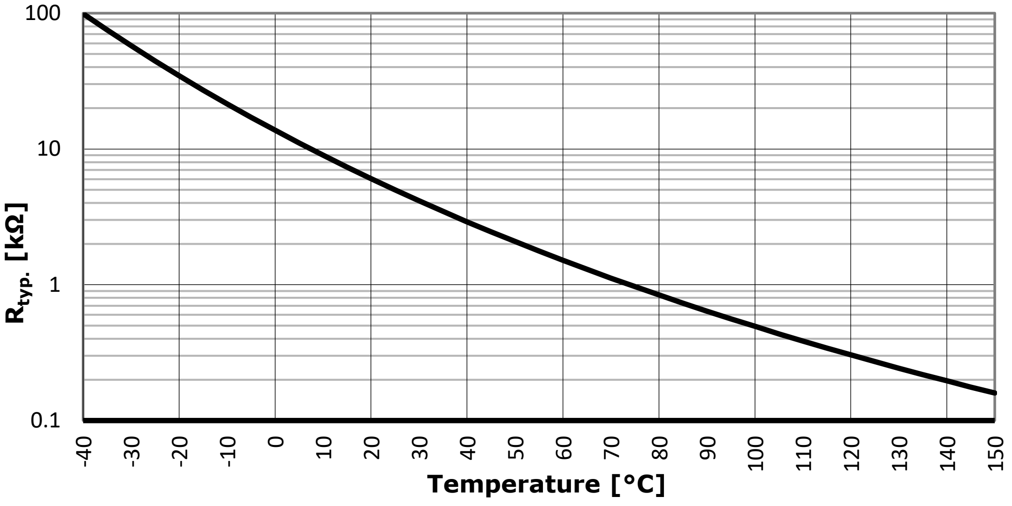
Table 4: NTC general equation and main parameters

$$R_2 = R_1 \cdot e^{\left[B_{(T_1/T_2)}\cdot\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right]}$$

R_2 : resistance at absolute temperature T_2 [K]
R_1 : resistance at absolute temperature T_1 [K]
B : B-value $B_{(T1/T2)}$ [K]

Symbol	Tolerance	min	typ	max	Unit
R_{25}	±5%	4.75	5.00	5.25	kΩ
R_{100}	±5%	468	493	518	Ω
$B_{(25/50)}$			3375		K
$B_{(25/85)}$			3420		K
$B_{(100/125)}$			3550		K

Figure 6: Typical NTC characteristic



1.7.2 Electrical insulation

Since the SEMITOP® module is filled with silicone gel for insolation purposes, the requirements for the specified insulation voltage (AC/2.5kV/1 min, AC/3kV/1s at 50Hz) are met and 100% tested.
Nevertheless, insulation properties may be endangered when short circuit failure and/or electrical overstress occur. The reason is that, during such failure events, the bond wires on the chips could melt off and generates an arc with high energy plasma. In this case, the direction of plasma expansion is not predictable and the temperature sensor may be touched by plasma thus exposed to a high voltage.
The safety grade "Safe electrical insulation" according to EN 50178 can be achieved by different additional means, described there in detail.

1.8 Thermal performance

The increase of power density, introduced by latest chip technology, in combination with request of longer lifetime, make thermal performance more and more important for a power module. SEMITOP®E1/E2 have been designed to fulfil such requirements and offer very low thermal resistance. 20 years expertise on SEMITOP® Gen1 brought to life an optimized pressure system, which is the best trade-off between mechanical robustness, thermal performance and cost.

For a given chip size, main factors affecting thermal performance of a chip are:

1.8.1. Properties and thickness of the materials between chip and heatsink
1.8.2. Contact between module and heatsink

Since property of the materials mainly depend upon state of the art technology, currently available on the market, what really makes SEMITOP®E1/E2 apart is the design principle, improving contact between module and heatsink.

1.8.1 Properties and thickness of materials between chip and heatsink

Thermal performance of a module are strongly dependent upon material between chip and heatsink. As general rule, the more the worse. SEMITOP®E1/E2 is a baseplate-less module; therefore, compared to modules having an additional copper baseplate, it leads to huge benefits, in terms of $R_{th(j-s)}$ and cost. Figure 7 provides an immediate view of the difference.

Figure 7: Thermal resistance breakdown (baseplate vs. baseplate-less)

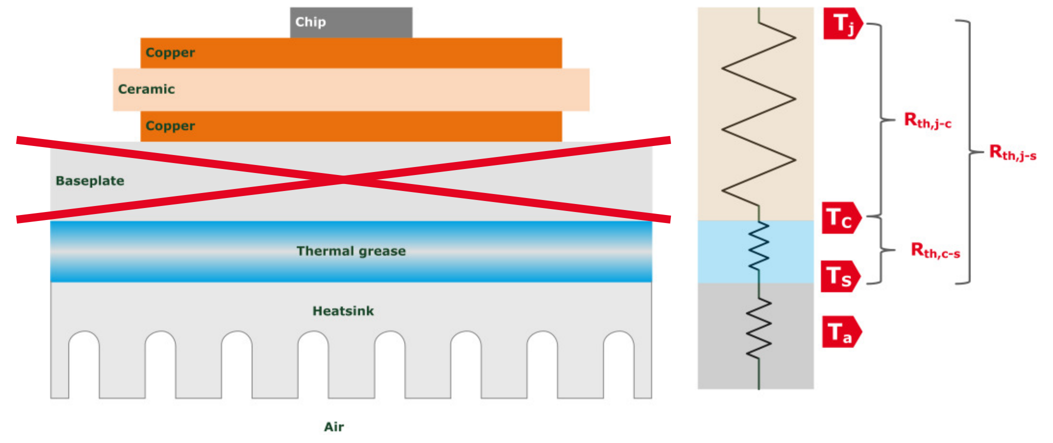


Table 5 below gives a detailed cross-section overview of thicknesses and thermal properties of all the materials between chip and heatsink (TIM excluded). Information about some chips technologies are given as an example, details related to a specific product (chips, layout) can be provided upon request.

Table 5: Typical material data for thermal simulations

Layer	Material	Layer thickness [µm]	Spec. Thermal conductivity λ @25°C [W/(m*K)]	Spec. Thermal Capacity @25°C [J/(kg*K)]	Density @25°C [kg/m^3]
1200V IGBT T7	Si	112	148	700…750	2330
1200V CAL4F diode	Si	261	148	700…750	2330
1600V PEP Net diode	Si	310	148	700…750	2330
Chip solder layer	SnAg	~100	57	214	7800
DBC Copper (top)	Cu	300	394	385	8960
DBC Ceramic	Al_2O_3	380	24	830	3780
DBC Copper (bottom)	Cu	300	394	385	8960
Thermal Interface Material (TIM)	Customer specific				

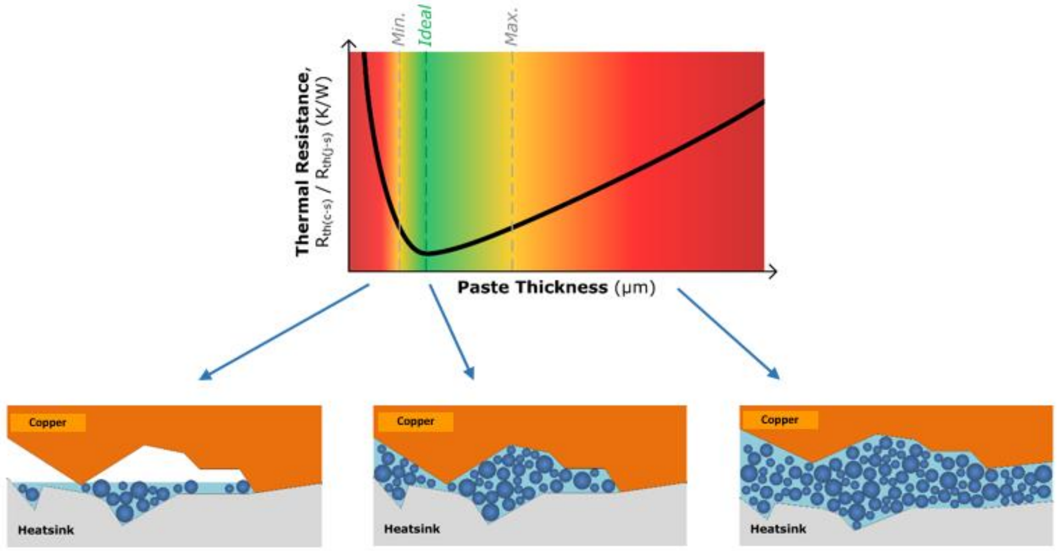
*) Alternative materials are also available and can be evaluated on project basis

Materials negatively influencing Rth(j-s) the most, are ceramic and TIM. Again, while thickness and material of ceramic layer has to be selected according to technology currently available on the market, thickness of TIM layer is a design factor and can be reduced only with proper design of the module.

1.8.2 Contact between module and heatsink

Contact between bottom copper of the module and heatsink is one of the most important factor affecting thermal resistance of a chip. Best thermal performance is achieved when metal-to-metal contact between copper and heatsink occurs. Unfortunately, this is an ideal condition which does not occur over the entire interface, because copper and heatsink have a natural warpage and always have a certain level of roughness. The function of the Thermal Interface Material (TIM) is to flow according to the shape of the interface and fill all gaps, enabling a metal-to-metal contact wherever this is possible. Therefore, a surplus of TIM is harmful as it reduces metal-to-metal contact and just introduces an additional layer of material between chip and heatsink. This means, in order to achieve best thermal performance, the amount of TIM must be optimized. SEMITOP®E1/E2 are designed for the usage of the minimum thickness of TIM layer as shown in Figure 8b.

Figure 8: Relationship between paste thickness and thermal resistance

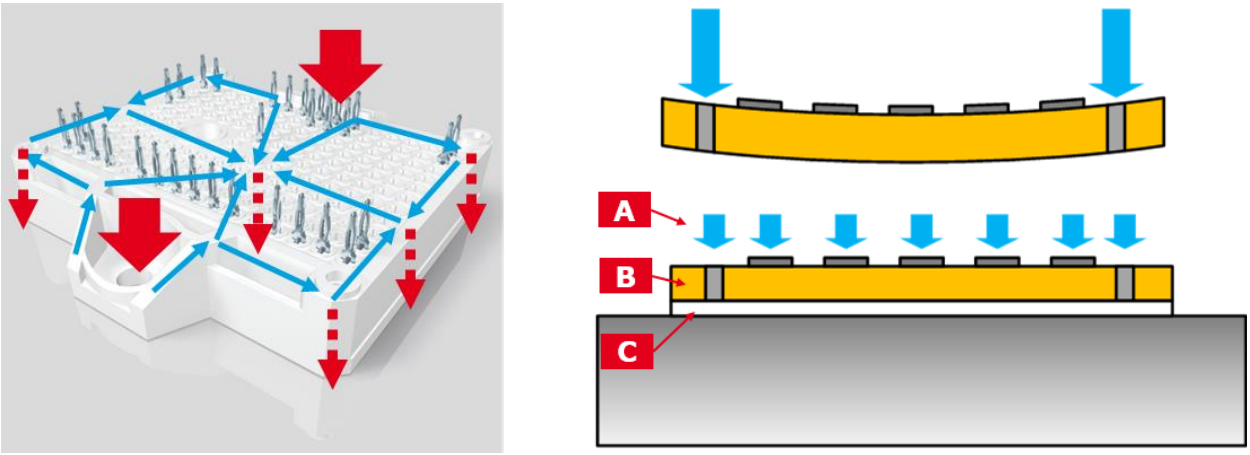


a) b) c)

Key features of SEMITOP®E1/E2 construction principle:

- Rigid design of the housing (Figure 9a), enabling to transfer more force from mounting point to entire DCB substrate.
- Convex shape of DCB substrate (Figure 9b), enabling:
  - A. Even pressure over entire DCB
  - B. Reduced warpage of DCB (after mounting)
  - C. Even TIM spread (after mounting)

Figure 9: Construction principle



a) b)

Thanks to this concept, SEMITOP®E1/E2 provides 20% lower $R_{th(j-s)}$ compared to industrial standard design. This allows more power out of same chip or, at same power, to reduce junction temperature, increase efficiency and extend chip lifetime. On top of this, SEMIKRON also offers an exclusive High Performance Thermal Paste (HPTP) which enables to further reduce $R_{th(j-s)}$ of additional 20%.

1.9 Thermal Interface Materials (TIM)

All SEMITOP®E1/E2 modules are available with pre-applied TIM:

- HPTP (High Performance Thermal Paste)
- PCM (Phase Change Material)

Further information about TIM and Mounting Instruction can be found on website:

- Technical explanation of TIM
- General guidelines on TIM application
- Mounting Instructions of SEMITOP®E1/E2

The typical $R_{th(j-s)}$ values, shown into SEMITOP®E1/E2 datasheets, are valid for modules assembled on the heatsink according to Mounting Instructions of SEMITOP®E1/E2, and following TIM:

- WP12 (λ_{paste} = 0.8 W/(mK))
- HPTP (λ_{paste} = 2.5 W/(mK))

2. Packaging specification

2.1 Packaging

SEMITOP®E1/E2 modules are packed into ESD (not electrically chargeable) blisters (Figure 10a and 10b) stored in a standard paper box (Figure 10c). Each box contains double layer of modules, safely held by sandwich blister (bottom + cover tray).

Figure 10: Packaging system

a) SEMITOP®E1 (425 x 320 x 21.2 mm^3)

b) SEMITOP®E2 (425 x 320 x 21.2 mm^3)

c) Paper box (same for SEMITOP®E1 and SEMITOP®E2)
(452 x 328 x 56 mm^3)

Quantities per package depend on module size as per following table:

Table 6: Number of modules per package

SEMITOP®E1	28x modules/blister x 2x blisters/box = **56x** modules/box
SEMITOP®E2	20x modules/blister x 2x blisters/box = **40x** modules/box

Two labels can be found on paper box (Figure 10c):

- **Yellow label**: warning for electrostatic sensitive devices.
- **White label**: information about product. Details about label content can be found here:
  - Labeling of SEMIKRON product packaging

Products with pre-applied TIM have additional labelling. Details can be found on website:

- Technical Explanation of TIM

2.2 Storage and shelf life conditions

SEMITOP® E products are qualified according to IEC 60721-4-1 and can be stored in original package under following storage conditions:

Table 7: Storage conditions	
Duration	2 years
Climatic class	1K2 (IEC 60721-3-1)

Following shelf life conditions, which are not tested but based on SEMIKRON experience, are possible and should not be exceeded:

Table 8: Shelf life conditions	
Relative humidity	Max. 85%
Storage temperature	-25°C … +60°C
Condensation	Not allowed at any time
Storage time	Max. 2 years

Different shelf life conditions may apply for modules with pre-applied TIM. Details can be found on website:

- ➢ Technical Explanation of TIM

3. Reliability

3.1 Qualification tests

The following tests are minimum requirements for the product release. Tests are being executed for release and re-qualification of new and/or re-developed modules. The scope of testing might be extended by further product-specific reliability tests.

Table 9: Qualification program

Test Description	Conditions
High Temperature Reverse Bias (HTRB) IEC 60747-9:2007	1000h
	95% $V_{CE\ max}$
	$T_{j\ max}$
High Temperature Reverse Bias (HTRB) * IEC 60747-2:2016	1000h
	66% V_{RRM}
	$T_s = T_{j\ max} - 20K$
High Temperature Gate Stress (HTGS) IEC 60747-9:2007	1000h
	$\pm V_{GES\ max}$
	$T_{j\ max}$
High Humidity High Temperature Reverse Bias (H3TRB) EN 60749-5:2018, EN 60068-2-67:1996	1000h
	$T_a = 85°C$, RH = 85%
	V_{CE} = max. 80V
High Voltage - High Humidity High Temperature Reverse Bias (HV-H3TRB) ** EN 60749-5:2018	1000h
	$T_a = 85°C$, $R_H = 85\%$
	80% $V_{CE\ max}$
High Temperature Storage (HTS) EN 60068-2-2:2008, IEC 60749-6:2002	1000h
	$T_{stg\ max}$
Low Temperature Storage (LTS) EN 60068-2-1:1993 + A1:1993 + A2:1994	1000h
	$T_{stg\ min}$
Thermal Cycling (TC) EN 60068-2-14:2010	100 cycles
	$T_{stg\ max}$ - $T_{stg\ min}$
Vibration IEC 60068-2-6:2008	20Hz … 500Hz Sinusoidal sweep
	5g
	2h per axis (x, y, z)
Mechanical Shock IEC 60068-2-27:2010	Half sine pulse 18ms
	30g
	3 times each direction (±x, ±y, ±z)
Power Cycling (PC) EN 60749-34:2010	>70k cycles at ΔT= 70K

*) Valid for standard glass passivated rectifier diodes and thyristors.
**) Valid for latest chip technology like Generation 7 IGBT "T7" and Planar Gen3 SiC MOS "CR03".

SEMITOP® modules can be subjected on demand to additional tests, as follows.

- Salt Spray Test according mil-std-810F method 509.4 +JESD22-a107-a
- Corrosive Atmosphere test according to DIN EN 60068-2-60Ke method 3 including SO_2 in addition to H_2S, NO_2 and Cl_2.

Test level may vary, depending on module layout and technology.

4. Index of figures and tables

4.1 Figures

4.2 Tables

5. Disclaimer

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