Technical Explanation
SKiiP® 4

SEMIKRON DANFOSS

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Prepared by:	Anastasia Schiller
Reviewed by:	Adyatmika Darmanandana
Approved by:	Daniel Prindle

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1. Related documents 3
2. Introduction 3
2.1 Heat Sink 5
2.2 Power Section 5
2.3 Gate Drive Unit 5
3. Topologies and Selection Guide 6
3.1 Type Designation Code 6
3.2 Overview of the available types and current ratings 7
4. Standards and Qualification Tests 8
4.1 Tests for qualification and re-qualification 8
4.2 Electromagnetic compatibility (EMC) 8
4.3 Isolation coordination 9
4.4 Installation Altitude 9
5. Gate Driver Board 13
5.1 Overview 13
5.2 Gate driver interface "SKiFace" 14
5.2.1 Overview 14
5.2.2 Pin description 15
5.2.3 External Power Supply 18
5.2.4 Switching Signal Inputs 19
5.2.5 Analog Output Signals 20
5.2.6 HALT Logic Signal 22
5.2.7 CMN_GPIO1 signal 24
5.2.8 CANbus interface 25
5.2.9 Ground Connection 26
5.2.10 Shield and protective earth/chassis connection 26
5.2.11 Reserved or not used signals 27
5.3 Digital signal transmission 29
5.4 Power-On-Reset 29
5.5 Interlock Dead Time Generation 30
5.6 Short pulse suppression 30
5.7 IntelliOff 31
5.8 Error Management 33
5.8.1 Error delay time, $t_{d(err)}$ 33
5.8.2 Under Voltage Protection (UVP) supply voltage 33
5.8.3 Exceeding the maximum switching frequency 33
5.8.4 Overlapping of switching signals 34
5.8.5 Over current Protection (OCP) 35
5.8.6 Short Circuit Protection (SCP) 35
5.8.7 Thermal protection (over temperature protection) 36
5.9 Analogue signals / sensor functionality 36
5.9.1 Load current sensor 36
5.9.2 Integrated DCB-temperature sensor 39
5.9.3 DC-Link Voltage Sensing 41

6. Power terminals 43
6.1 Electrical limits 43
6.2 Torque at terminal connections 43
6.3 Mechanical constraints 44
7. Application hints 45
7.1 Verification of design 45
7.2 Safe Operating Area for SKiiP 4 45
7.3 Maximum blocking voltage and snubber capacitors 46
7.4 Definition of Thermal Resistance 46
7.5 Cooling and coolant circuit 48
7.5.1 Prerequisites 48
7.5.2 Materials used and fluid composition 48
7.5.3 Water connection description of water-cooled SKiiP 4 49
7.6 Isolation voltage test (IVT) 50
7.7 FRT (Fault Ride Through) - Function 52
7.8 Solar function 54
7.9 Recommended temperature rating 56
7.10 Switching operation and current sharing between paralleled half bridge modules 58
7.11 Paralleling of SKiiP®4 59
7.12 Prevention of condensation 61
8. Logistics 62
8.1 Label 62
8.1.1 System Label 62
8.1.2 Half-Bridge Laser Label 62
8.1.3 Warranty Label 62
8.1.4 Matrix Code 63
8.1.5 Provisions and handling after use 63
9. Abbreviations 66
10. Symbols 67

Please note:
Unless otherwise specified, all values in this technical explanation are typical values. Typical values are average values derived from large quantities of tested SKiiPs and are provided for information purposes only, thus, they're not a binding specification. These values can and do vary under different application conditions. All operating parameters must be validated by the user's technical experts for each application.

This document is valid for the following SKiiP 4 product range:

1200V:

SKiiP1814GB12E4-3D…

SKiiP2414GB12E4-4D…

SKiiP3614GB12E4-6D…

1700V:

SKiiP1814GB17E4-3D…

SKiiP2414GB17E4-4D…

SKiiP3614GB17E4-6D…

followed by U oder PV followed by W, L, LR or HP with the following part numbers 20601xxx, 20602xxx, 20603xxx and 20604xxx

This technical explanation document is valid as well for customized SKiiP 4 with part numbers 20601xxx, 20602xxx, 20603xxx and 20604xxx with product name SKiiPxxxxGBxxxx-xDUKxxx excepting restrictions or features which are subject of a customized specification.

The document remains effective until replaced by a subsequent revision of this document.

1. Related documents

- Datasheets SKiiP 4
- Diagnostic Interface SKiiP 4 – CANopen User Manual
- Technical Explanation SKiiP 4 Parallel Board
- Technical Explanation SKiiP 4 F-Option
- Technical Explanation SKiFace Adapter Board

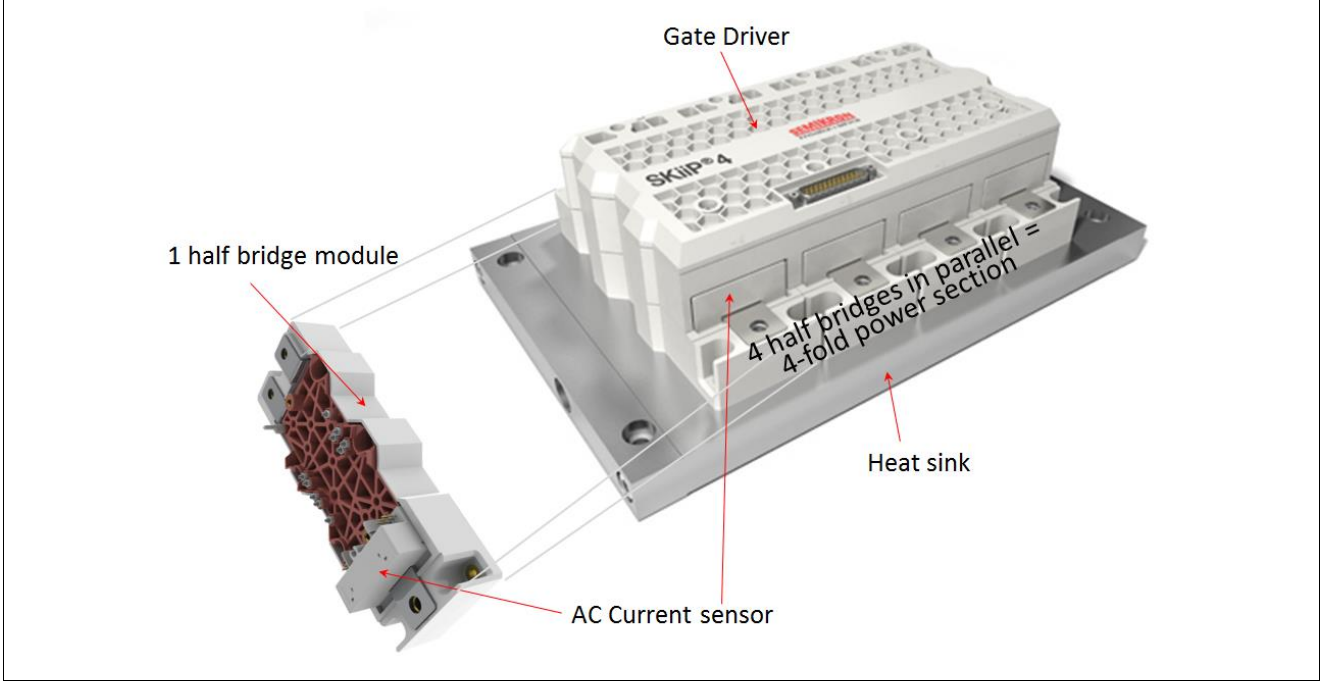
All these documents can be found on the SEMIKRON Danfoss internet page (www.semikron-danfoss.com) or requested at Semikron Danfoss

2. Introduction

The 4th generation SKiiP "SKiiP®4" is an Intelligent Power Module (IPM) with highest power density and reliability. SKiiP stands for "SEMIKRON Danfoss intelligent integrated Power" indicating that four components are integrated into one IPM:

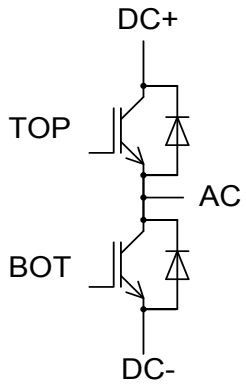
- Heat sink
- Power stage
- Gate drive and protection circuitry
- Current sensor

Figure 1: SKiiP 4 – 4 fold



The power section consists of 3, 4 or 6 parallel connected half bridge modules whereas a half bridge is defined in Figure 2. The exploded assembly view of a half bridge module is shown in Figure 3. As convention the IGBT and the diode connected between DC+ and AC are named TOP IGBT and TOP diode respectively. Consequently, the IGBT and the diode between AC and DC- are named BOT IGBT and BOT diode respectively.

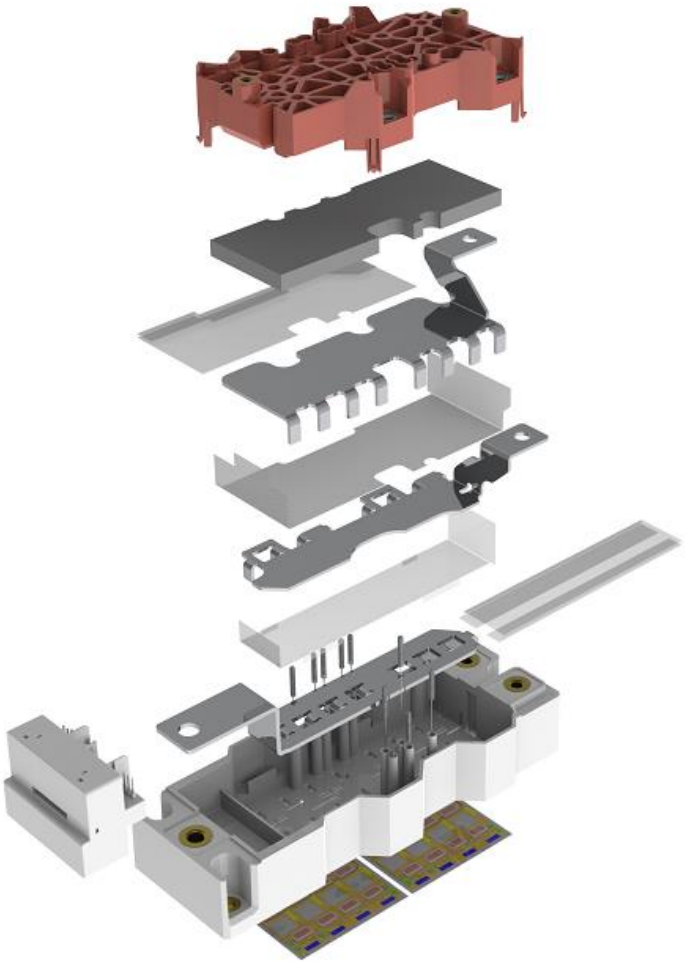
Figure 2: Half bridge definition



In this document following synonyms will be used for a power section with

- 3 half bridge modules in parallel = 3-fold
- 4 half bridge modules in parallel = 4-fold
- 6 half bridge modules in parallel = 6-fold

Figure 3: Half bridge "exploded assembly view"



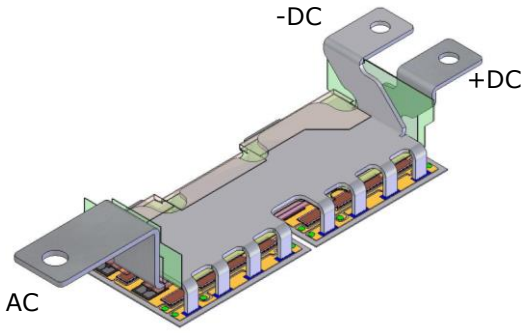
2.1 Heat Sink

Semikron Danfoss offers highly efficient water-cooled heat sinks and air cooled aluminum heat sinks. Detailed technical parameter is given in the datasheet of the corresponding SKiiP. Customer specific heat sinks can be designed, simulated, measured, and assembled on request as well. Suitable design rules should be followed to create such a custom specific. Please refer to the PI 12-034 for such detailed information and get in touch with your local Semikron Danfoss representative in case further assistance is required.

2.2 Power Section

The SKiiP 4 power section is constructed utilizing pressure contact technology and without a copper base plate, e.g. the SKiiP 4 is a "baseplate less" module. Thus, the pressure to attach the substrate to the heatsink is homogenously induced by a dedicated pressure part on top, which is screwed to the heat sink. The pressure contact technology facilitates that the Al_2O_3 or AlN DCB (direct copper bonded) substrate is pressed directly onto the heat sink without the use of a base plate and only a well-defined minimum amount of thermal compound is required. Contact springs are used for all auxiliary signal connections between the substrate and the Gate Driver PCB like gates, auxiliary emitters and temperature sensor. These spring contacts allow solder-free connection of the driver PCB. The pressure system ensures that the pressure is evenly applied to the numerous contacts situated next the chips, thus, resulting in a very low thermal and Ohmic resistance $R_{CC'+EE'}$ (refer to Figure 4).

Figure 4: Main terminals construction principle



In the SKiiP 4 in contrast to previous generations of SKiiPs the bare chips are sintered and not soldered. The sophisticated sintering process is based on a pulverized silver which creates a robust material connection when suitable pressure and temperature is applied during the formation process. This sintering process connects the chip and DCB surface extremely stably up to the melting point of silver which is as high as 962°C.

Contact springs as mentioned before are used for all connections between substrate and Gate Driver PCB like for the gate, auxiliary emitter and temperature sensor. These spring contacts allow the solder-free connection of the driver board.

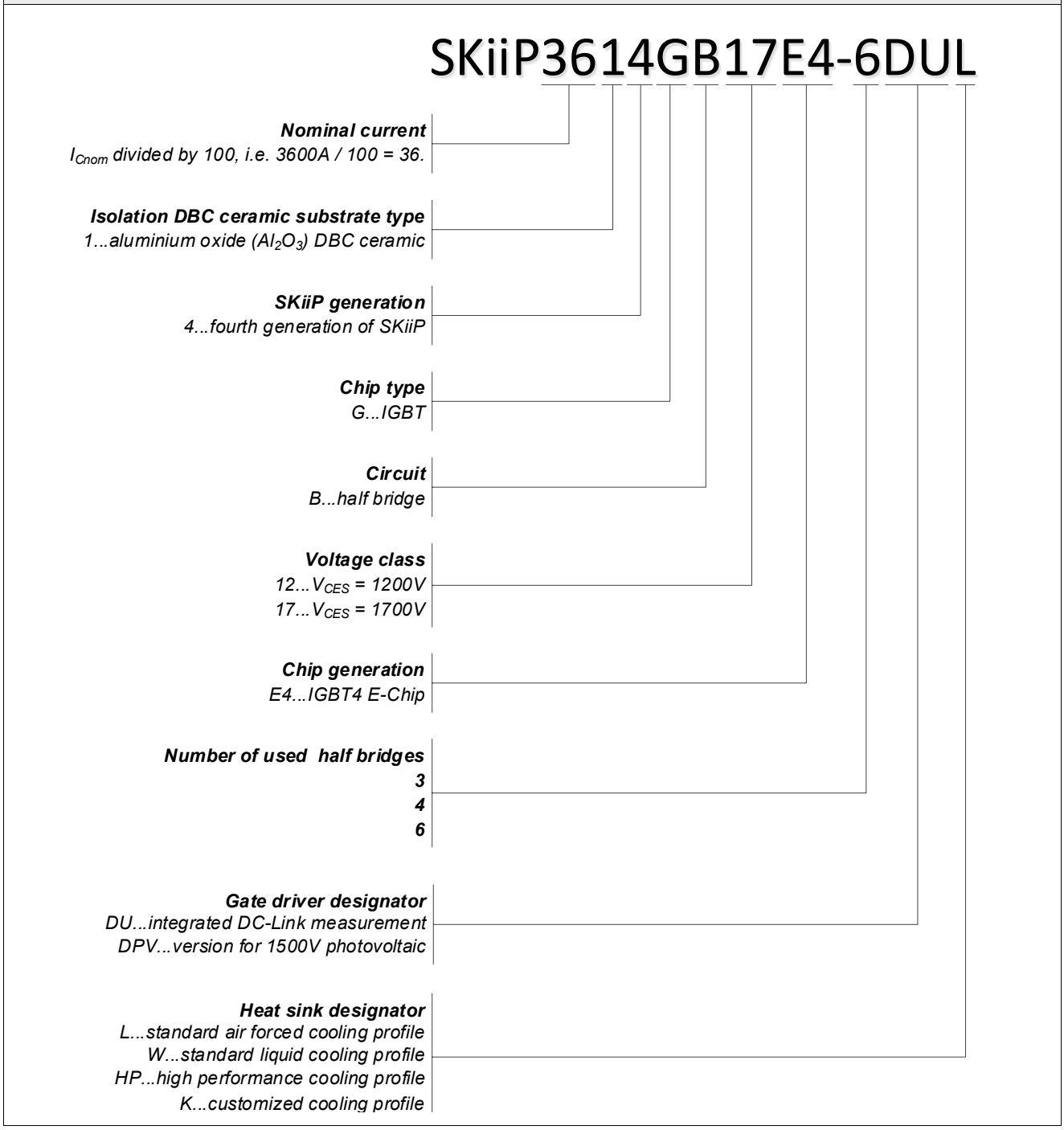
2.3 Gate Drive Unit

The Gate Driver Unit controls the behavior of the SKiiP under normal and exceptional operation. It receives, checks and conditions the input signals to further transform them into suitable output signals to control the gates of the employed IGBT. Furthermore, the Gate Drive Unit establishes a safe signal insulation between high and low voltage sides of the driver board. Additionally, the gate drive circuit ensures a proper handling of fault conditions as well as turning-off the IGBT safely even under exceptional conditions like short circuit etc. The SKiiP 4 employs various user accessible parameter to configure and customize certain parameter like threshold values through the integrated CANbus interface. Among those functions is an error storage, too providing extended information as required for a detailed failure analysis.

3. Topologies and Selection Guide

3.1 Type Designation Code

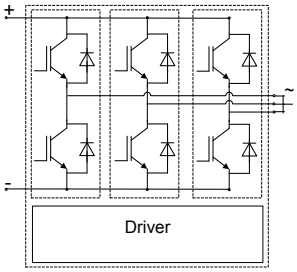
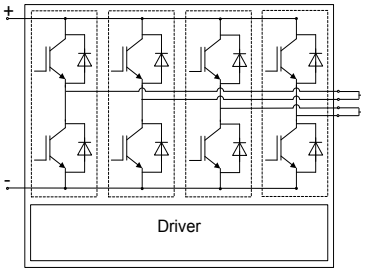
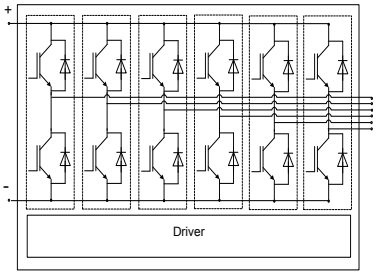
Figure 5: Type Designation Code



3.2 Overview of the available types and current ratings

Error! Reference source not found. Table 1: SKiiP 4 standard product range and corresponding current ratings (I_{Cnom}).

Table 1: SKiiP 4 standard product range

3-fold		4-fold		6-fold	
					
SKiiP 1814GB12E4-3DUW/HP	SKiiP 1814GB17E4-3DUW/HP	SKiiP 2414GB12E4-4DUW/HP	SKiiP 2414GB17E4-4DUW/HP	SKiiP 3614GB12E4-6DUW/HP	SKiiP 3614GB17E4-6DUW/HP
					
SKiiP 1814GB12E4-3DUL	SKiiP 1814GB17E4-3DUL	SKiiP 2414GB12E4-4DUL	SKiiP 2414GB17E4-4DUL	SKiiP 3614GB12E4-6DUL	SKiiP 3614GB17E4-6DUL
					
I_{Cnom} = 1800A		I_{Cnom} = 2400A		I_{Cnom} = 3600A	

4. Standards and Qualification Tests

4.1 Tests for qualification and re-qualification

Table 2: SKiiP 4 Tests for qualification and re-qualification			
No	**Test**	**Test Conditions**	**Standard**
01	High Temperature Reverse Bias	1000h, V_{GE} = 0V, 95% V_{CEmax} T_s=T_{jmax}-10°C	IEC 60747-9
02	High Temperature Gate Stress	1000h, +/- V_{GEmax}, T_{jmax}	IEC 60747-9
03	High Humidity High Temperature Reverse Bias	1000h, 85°C, 85% RH, $V_{CE\ max.}$=1360 V, V_{GE}=0V	IEC 60068 Part 2-67
04	High Temperature Storage	1000h, T_a = +125°C	IEC 60068 Part 2-2
05	Low Temperature Storage	1000h, T_a = -40°C	IEC 60068 Part 2-1
06	Thermal Cycling	100 cycles, -40°C/ +125°C	IEC 60068 Part 2-14
07	Power Cycling (EOL-Test)	60.000 load cycles @ ΔT_j = 110K, T_{jm}=95°C 200.000 load cycles @ ΔT_j = 70K, T_{jm}=115°C	IEC 60747-9
08	Vibration (Halt Test)	Sinusoidal Sweep, 5g, x, y, z – axis, 2h/ axis	IEC 60068 Part 2-6
09	Shock (Halt Test)	Half-sinusoidal Pulse, 30g, +/- x, +/- y, +/- z direction, 1000 times per direction	IEC 60068 Part 2-27
10	Corrosive gas test	T_a = 25°C, 75%RH, 4 components: H_2S (hydrosulphide), NO_2 (nitrogen dioxide), Cl_2 (Chlorine), SO_2 (Sulphur dioxide), 21 days	IEC 60068 Part 2-60

4.2 Electromagnetic compatibility (EMC)

The SKiiP 4 is designed to withstand the following immunity tests with EMC compliant installation:

Table 3: SKiiP 4 Electromagnetic compatibility		
Immunity test	**Conditions**	**Test level**
Fast transients (Burst) (61000-4-4)	On driver board interfaces	4kV / 5kHz
Radio Frequency Fields (61000-4-3)	Polarisation: vertical + horizontal Frequency: 80 MHz - 1000 MHz Modulation: 80% AM, 1kHz Far field, homogeneous Stripline acc.11425-5 level III/F3	 20V/m 200V/m
RF Conducted Disturbance (61000-4-6)	Frequency: 150 kHz - 80 MHz Modulation: 80 % AM, 1kHz	Voltage: 20V EMF
Magnet field (61000-4-8)	Far field, homogeneous	170A/m
Electrostatic discharge (ESD) EN 61000-4-2	Contact discharge Air discharge	6kV 8kV

4.3 Isolation coordination

The isolation of the SKiiP 4 is designed according to EN50178 and EN61800-5-1. For working conditions, please refer to the datasheet SKiiP 4. 20601xxx and 20602xxx.

Table 4: : SKiiP 4 Isolation limits		
Isolation / Test level	Min value	
Creepage primary - secondary	14mm	
Creepage secondary – heat sink potential	8mm	
Clearance primary – secondary	14mm	
Clearance secondary – heat sink potential	8mm	
Partial discharge extinction voltage (IEC60664-1) between primary and secondary side of driver board	1900V rms; Q_{PD} < 10pC	
Rated surge withstand voltage (IEC60664-1) primary to secondary primary to heat sink	Part.Nr: 20601xxx 8kV 8kV	Part.Nr: 20602xxx 12kV 8kV

4.4 Installation Altitude

Isolation coordination for SKiiP 4 is designed for overvoltage category III and for altitudes of up to 2000m.

The required clearance distances between mains-circuits and their environment for overvoltage category III are listed in EN50178.

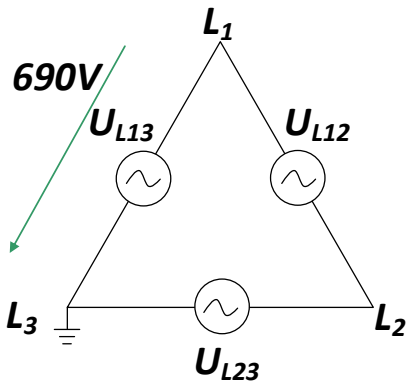
For an earthed-neutral system the rated isolation voltage is defined in chapter 5.2.16.1 of EN50178 as:

"…the peak value of the rated voltage between phase and earthed neutral point."

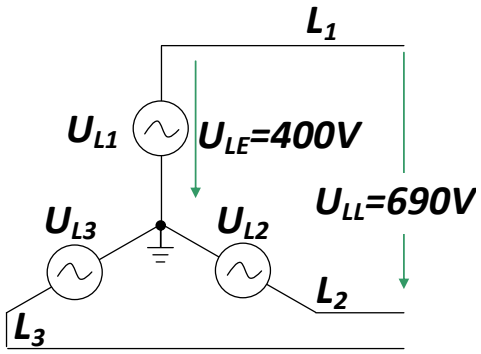
Based on this standard sentence the rated isolation voltage in case of a grounded delta grid and a star grounded grid can be derived as:

- Rated isolation voltage in case of 690V grounded delta grid: 690V
- Rated isolation voltage in case of 690V star grounded grid: 400V

Figure 6: Schematics of Grounded Delta Grid and Star Grounded Circuit Network



Grounded delta grid



Star grounded circuit network (690V-TN-grid)

Based on the type of grid and the voltage level the required clearance distance for basic and reinforced isolation can differ from the designed ones.

According to HD625 S1 and IEC60664-1 the maximum altitude can be calculated based on the factors between required and designed clearance distances.

Table 5: Altitude Correction Factors (IEC 60664-1)		
Altitude [m]	**Normal barometric pressure [kPa]**	**Multiplication factor for clearances**
2 000	80,0	1,00
3 000	70,0	1,14
4 000	62,0	1,29
5 000	54,0	1,48
6 000	47,0	1,70
7 000	41,0	1,95
8 000	35,5	2,25
9 000	30,5	2,62
10 000	26,5	3,02
15 000	12,0	6,67
20 000	5,5	14,5

The overvoltage category influences the installation altitude, too. In order to increase the installation altitude further the overvoltage category needs to be reduced (EN50178):

"*As an alternative to the values of table 3, columns 2 to 5 (of the cited standard), the clearance between mains-circuits of an EE and its environment may be designed in accordance with overvoltage category II, if facilities are provided which reduced overvoltages of category III to values of category II…However for reinforced isolation according to column 7 (of the cited standard) shall* ***not*** *be reduced.*"

The required clearance distances between mains-circuits and their environment for overvoltage category II are listed in EN50178.

If safety isolation is necessary the maximum altitude of SKiiP 4 is 6250 m (690 TN grid and overvoltage category II).

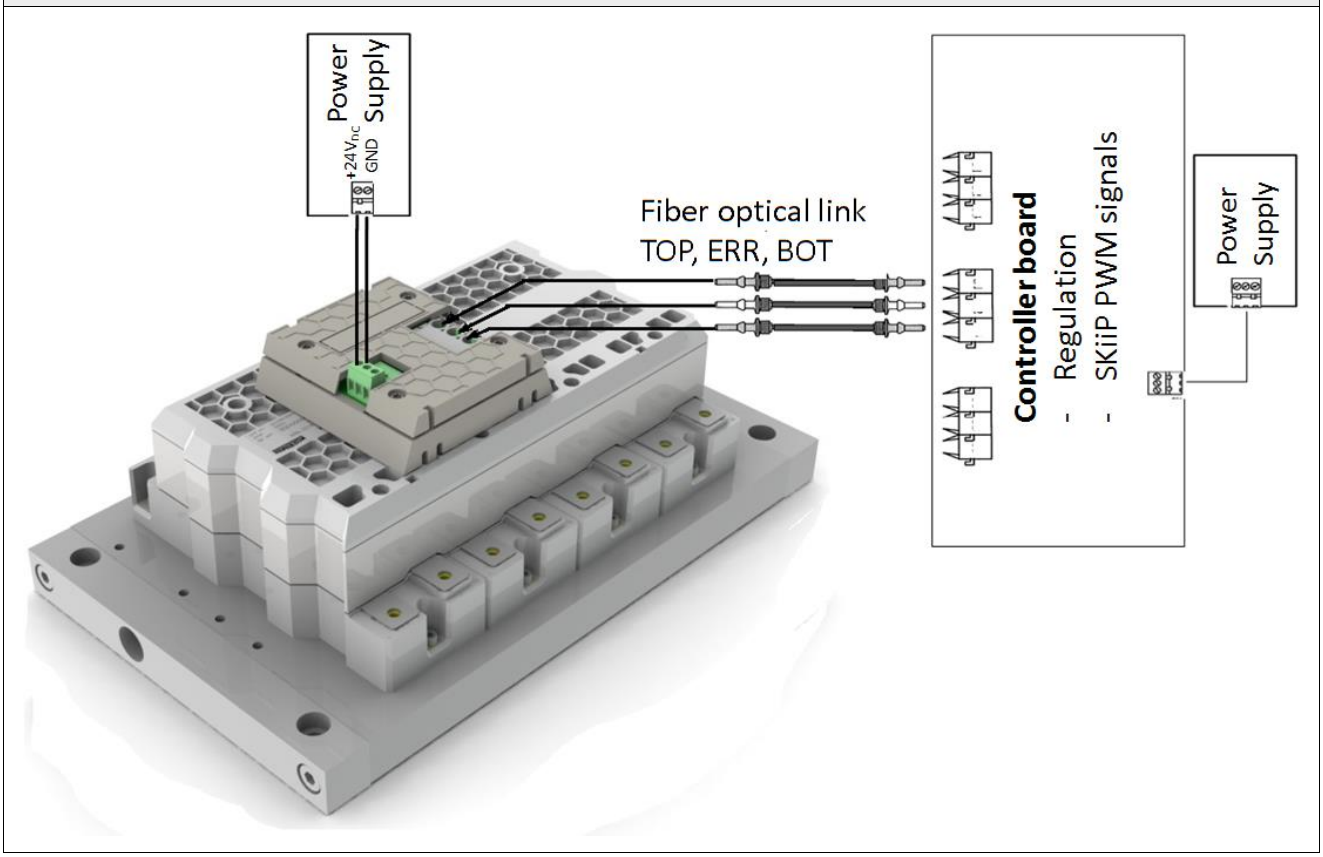
If only basic isolation is required even higher operation altitudes are possible. In case of a 690V TN grid and overvoltage category II an altitude of theoretically 9000 m for SKiiP 4 is possible.

This is the case when an additional basic isolation is implemented between the SKiiP 4 driver interface and controller board. This can be realized by the following means:

- Use of fiber optic for control signals (TOP, BOT, Error) **and**
- SKiiP analogue signals (current, DC-voltage and temperature measurement) are not used **and**
- all SKiiPs are supplied by separate power supplies to which no other circuit is connected.

The above described implementation is shown in Figure 7. The "F-Option board" for an optical fibre based isolation of the SKiiP 4 can be ordered separately and can be easily mounted on the SKiiP 4 top cover.

Figure 7: Implementation of additional basic isolation between SKiiP 4 driver interface and controller board

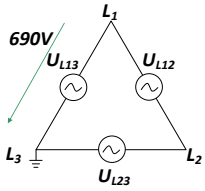
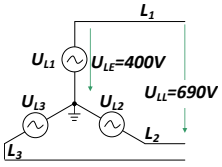
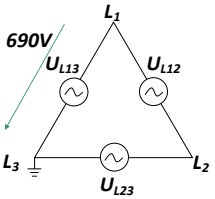
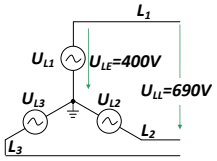


Finally, the installation altitude of the SKiiP 4 depends on:

- Grid configuration (star grounded grid, delta grounded grid)
- The voltage level of the line to earth voltage (rated isolation voltage)
- The overvoltage category (II or III)
- Whether safety isolation is required or not

Table 6 summarizes the installation altitudes for SKiiP 4.

Table 6: Installation altitudes for SKiiP 4 as function of the grid configuration, overvoltage category and required isolation degree

		Overvoltage category III		**Overvoltage category II**	
SKiiP4 (with 690V grounded delta)		Grounded delta grid	TN 690V	Grounded delta grid	TN 690V
					
Basic isolation against ground	Required for 2000m	8 mm	5.5 mm	5.5 mm	3 mm
	Existing	8 mm			
	Factor	1	1.45	1.45	2.66
	Altitude	**2000m**	**4840m**	**4840m**	**9000m**
Rein-forced isolation	Required for 2000m	14 mm	8 mm	14mm	8mm
	Existing	14 mm			
	Factor	1	1.75	1	1.75
	Altitude	**2000m**	**6250m**	**2000m**	**6250m**
Maximum Altitude with safety isolation		**2000m**	**4840m**	**2000m**	**6250m**
Maximum Altitude without safety isolation		**2000m**	**4840m**	**4840m**	**9000m**

5. Gate Driver Board

5.1 Overview

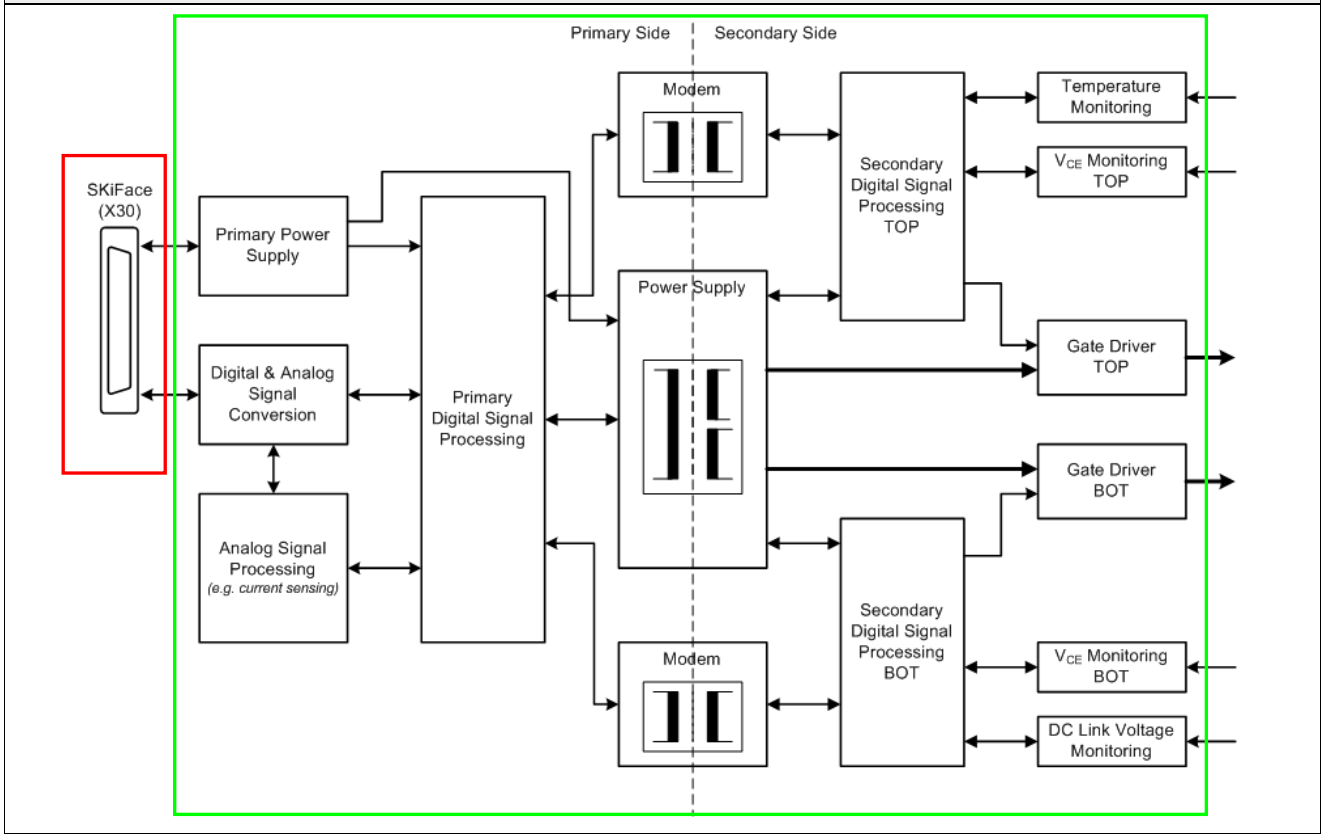
- The functionality of the Gate Driver board is indicated in the following block diagram in Figure 8.
- Gate driver interface SKiFace marked as red block (refer to Chapter 5.2)
- Gate driver board marked as green block.

The SKiiP 4 gate driver board includes the following functions:

- Digital signal transmission (refer to chapter 5.3)
- Power-on Reset (refer to chapter 5.4)
- Dead time generation (refer to chapter 5.5)
- Short pulse suppression (refer to chapter 5.6)
- IntelliOff switching (refer to chapter 5.7)
- Failure management (refer to chapter 5.8)

The driver is based on digital signal processing technology, which provides individual control parameter settings and the transmission of galvanic insulated sensor signals. The digital signal processing approach ensures high noise rejection. IGBT overvoltage especially during high current turn-off conditions are detected and reduced by the gate driver through an implemented function further called intelligent turn-off control circuit.

Figure 8: Gate Driver Board block diagram



5.2 Gate driver interface "SKiFace"

5.2.1 Overview

The Gate Driver Interface "SKiFace" is shown in the red colour marked frame of Figure 9. "SKiFace defines the 25 pin D-Sub male plug connector and the corresponding signal assignment. The appearance of the plug, its pin-out and dimensions are summarized in Figure 10.

The SKiFace interface provides pins for:

- External Power Supply (refer to chapter 5.2.3)
- Switching signal input (refer to chapter 5.2.4)
- Analogue signals (refer to chapter 5.2.5)
- HALT logic (refer to chapter 5.2.6)
- CMN_GPIO 1 output (refer to chapter 5.2.7)
- CMN_GPIO 2 (refer to chapter 5.7)
- CAN interface (refer to chapter 5.2.8)

Figure 9: Gate Driver Interface

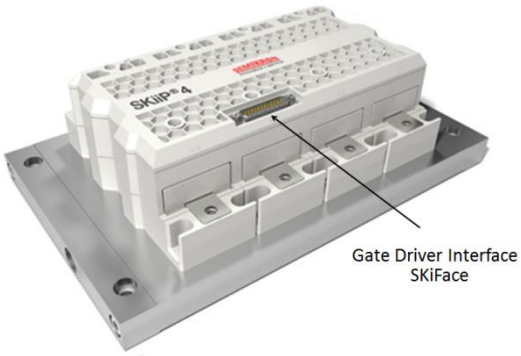
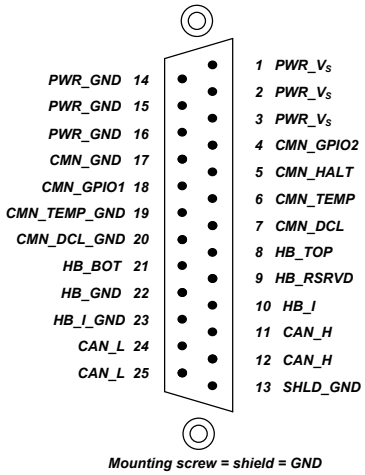
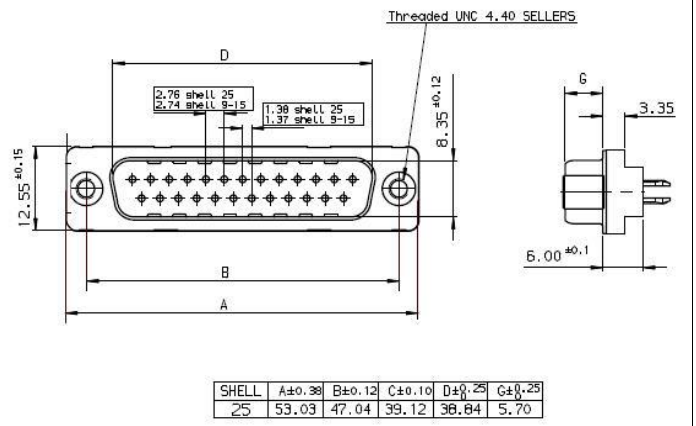


Figure 10: SKiiP 4 - connector D-Sub 25 pin, male plug, vertical, top view

Picture	Pin Configuration	Dimensions
		

SHELL	A±0.38	B±0.12	C±0.10	D±0.25	G±0.25
25	53.03	47.04	39.12	38.84	5.70

When connecting the SKiiP 4 to a control circuit the following recommendations shall be observed for a proper cable selection:

- Cable length should be kept shorter than 3m
- Utilization of shielded cables is recommended
- Longer cables must be shielded

A verification of mechanical stability and EMC behaviour under customer's application conditions is necessary.

As the SKiFace interface is a standardized, it is also used in other Semikron Danfoss products. Due to that not all signals are used for SKiiP 4.

An unused signal is: HB_RSRVD

Please note: The protective plastic cover of the D-Sub connector should be removed only just before the start of operation (ESD-Handling and protection)

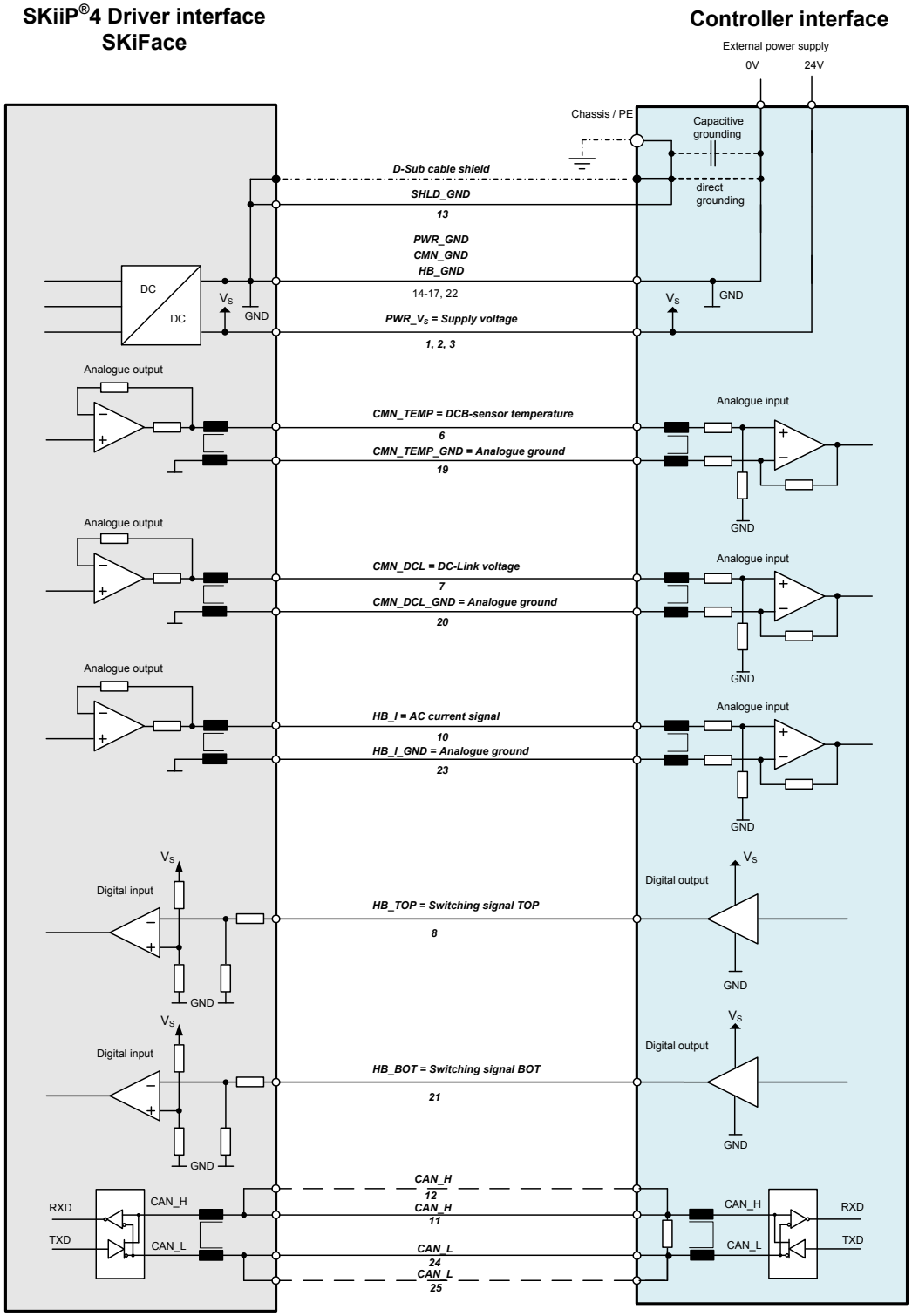
5.2.2 Pin description

Table 7: Pin configuration SKiiP 4

PIN	Signal	Function	Specification
1/2/3	PWR_VS	Power Supply	+24V (+/- 20%)
4	CMN_GPIO2	Digital input/ output Bidirectional status signal	Sync-signal for parallel operation (available after activation through CAN-bus message) For details see IntelliOff function, chapter 5.7
5	CMN_HALT	Digital input/ output Bidirectional status signal	LOW (dominant) = not ready to operate (e.g. error) HIGH (recessive) = ready to operate For details refer to HALT Logic Signal, chapter 5.2.6
6	CMN_TEMP	Temperature signal out	This pin is used to indicate the temperature sensor's analogue signal. Max output current: 5mA Nominal voltage range: 0 … +10V Refer to Integrated DCB-Temperature Sensor, chapter 5.9.2
7	CMN_DCL	DC-Link voltage out	This pin is used to indicate the DC-Link voltage level. Max. output current: 5mA Nominal voltage range: 0 … +10V For details refer to DC-Link-Voltage Sensing, chapter 5.9.2
8	HB_TOP	Switching signal input for high side IGBT	LOW = High side IGBT off HIGH = High side IGBT on For details refer to Switching Signal Inputs, chapter 5.2.4
9	HB_RSRVD	Reserved	Not connected
10	HB_I	Current sensor out	This pin is used to indicate the current sensor's analogue signal. Max. output current: 5mA Nominal voltage range: -10V … +10V For details refer to AC-current sensor, chapter 5.9.1
11	CAN_H	CAN interface INPUT/ OUTPUT HIGH	Input impedance = very high Specification according to ISO 11898.
12	CAN_H		Internally connected to pin 11
13	SHLD_GND	GND	Internally connected to PWR_GND
14/15/16	PWR_GND	Ground for PWR_VS	

17	CMN_GND	Ground for CMN_HALT, CMN_GPIO1/2	Internally connected to PWR_GND
18	CMN_GPIO1	Digital Input/Output General purpose IO	Inverted CMN_HALT signal (except in case of an activated FRT-function, please refer to chapter CMN_GPIO1 signal, chapter 5.2.7
19	CMN_TEMP_GND	Ground for CMN_TEMP	
20	CMN_DCL_GND	Ground for CMN_DCL	
21	HB_BOT	Switching signal input for low side IGBT	LOW = Low side IGBT off HIGH = Low side IGBT on For details refer to Switching Signal Inputs, chapter 5.2.4
22	HB_GND	Ground for CMN_HB_TOP, CMN_HB_BOT, CMN_HB_RSRVD	Internally connected to PWR_GND
23	HB_I_GND	Ground for HB_I	
24	CAN_L	CAN interface INPUT/ OUTPUT LOW	Input impedance = very high; Specification according to ISO 11898.
25	CAN_L		Internally connected to pin 24

Figure 11: Overview schematics SKiFace interface (CMN_GPIO1/2 and CMN_HALT are not shown



The left side shows the equivalent circuit diagram of the driver board with ground connections. The right side shows an application example of the controller side.

5.2.3 External Power Supply

Table 8shows the required features of an appropriate external power supply for a SKiiP 4.

Table 8: Requirements to the auxiliary power supply	
Power supply	The maximum ratings for the supply voltage are given in the SKiiP 4 data sheet on page 1 (refer to symbol Vs). The supply voltage is defined at the SKiiP 4 input, not at the controller output (voltage drop on connection cable)
Maximum rise time of 24V	<2 s
Rated current	1,5 times of the maximum driver input current
Minimum peak current	2 times of the maximum driver input current (At least 1.5A)

Please note: Do not apply switching signals during power up.

The external power supply requires the capability to feed a minimum inrush current into the SKiiP 4 at start-up of the system without entering a fault state itself. Typically power supplies with fold-back characteristic or hiccup-mode can create problems if insufficient over current margin is available. The voltage has to rise continuously and without any plateau formation.

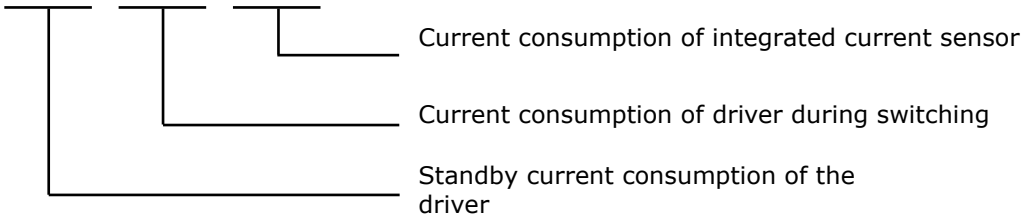
In order to ensure continuous operation and to have sufficient margin in case of overload it is recommended to select the rated current of the external power supply sufficiently higher than the SKiiP's maximum specified input current (see symbol Is on page 2 of the corresponding SKiiP 4 datasheet).

If the power supply is able to provide a higher current, a peak current will flow in the first instant to mainly charge the input capacitances on the driver. The peak current value will be limited only by the external power supply and the effective impedances (e.g. cabling etc-) as present in the connection between power supply and the SKiiP. It is recommended to avoid the paralleling of several customer side external power supply units. Their different current limitations may lead to drops in the supply voltage and unpredictable instable behaviour.

The formula given in the SKiiP 4 datasheet for calculating the supply current I_S (page 2) consists of three parts:

- The first part is the current consumption of the driver during standby. No switching signals are applied. Consequently, no AC-current is flowing. The example below is given for a SKiiP2414GB17E4 (I_{SO}=260mA).
- The second part is the required current consumption of the driver during switching.
- The third part is the current consumption required by the integrated current sensor to compensate the present value of the AC-current.

$$I_s = 260\,mA + k_1 \cdot f_{sw} + k_2 \cdot I_{AC}{}^2$$



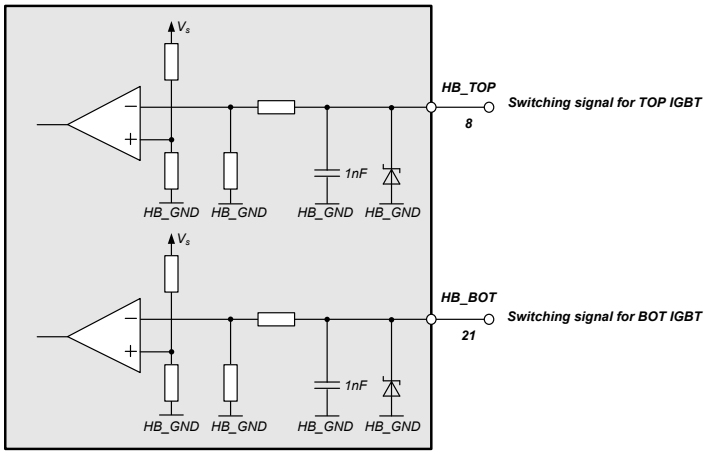
5.2.4 Switching Signal Inputs

The switching signal inputs HB_TOP for the TOP IGBT and HB_BOT for the BOT IGBT have a digital positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off) characteristic.

For driving the inputs HB_TOP and HB_BOT it is mandatory to use line drivers with a push-pull characteristic. Pull up and open collector output stages must not be used for driving these inputs. It is recommended to chose line drivers (e.g. IXDD604) according to the length of the signal wires.

Please note: A non-connected input will be considered as LOW signal.

Figure 12: TOP/BOT PWM Signal Input



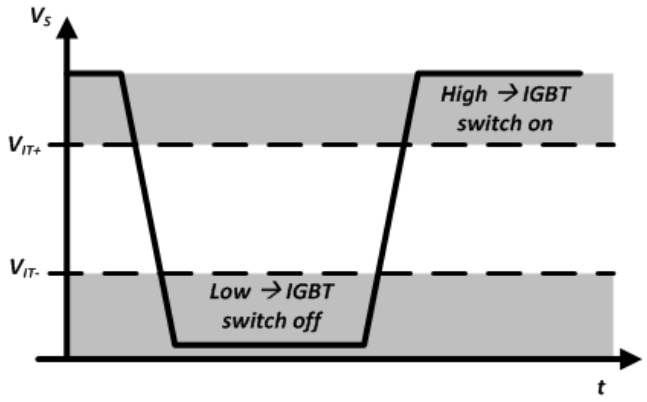
A 1nF capacitor is connected to the switching signal input to obtain high noise immunity. This capacitor can cause a delay of few ns for current limited line drivers, which can be neglected.

Input resistance is about 13kOhm

As shown figure below. the switching signal will be considered as:

- High when > V_{IT+}
- Low when < V_{IT-}

Figure 13: Threshold level for HB_TOP and HB_BOT



The threshold values V_{IT+} and V_{IT-} are given in the corresponding SKiiP 4 datasheet on page 2.

V_{IT+}: Minimum threshold that guarantees that input voltage level is recognized to switch on the IGBT.
V_{IT-}: Maximum threshold that guarantees that input voltage level is recognized to switch off the IGBT.

All threshold values are related to the supply voltage V_s.

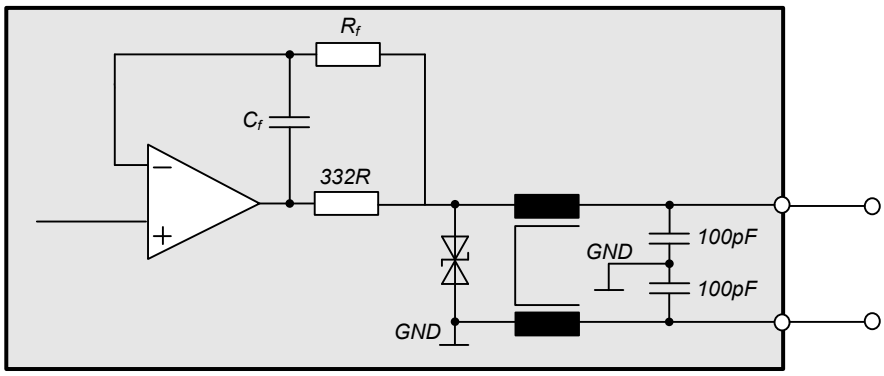
5.2.5 Analog Output Signals

The schematic in the Figure 14 shows the analogue output circuit of the gate driver.

This circuit is utilized in:

- Measurement of AC-current
- Measurement of DC-link voltage
- Measurement of DCB-sensor temperature

Figure 14: Schematic view of the analogue output signals



A resistor avoids damages potentially being caused by a temporary short circuit at the analogue output.

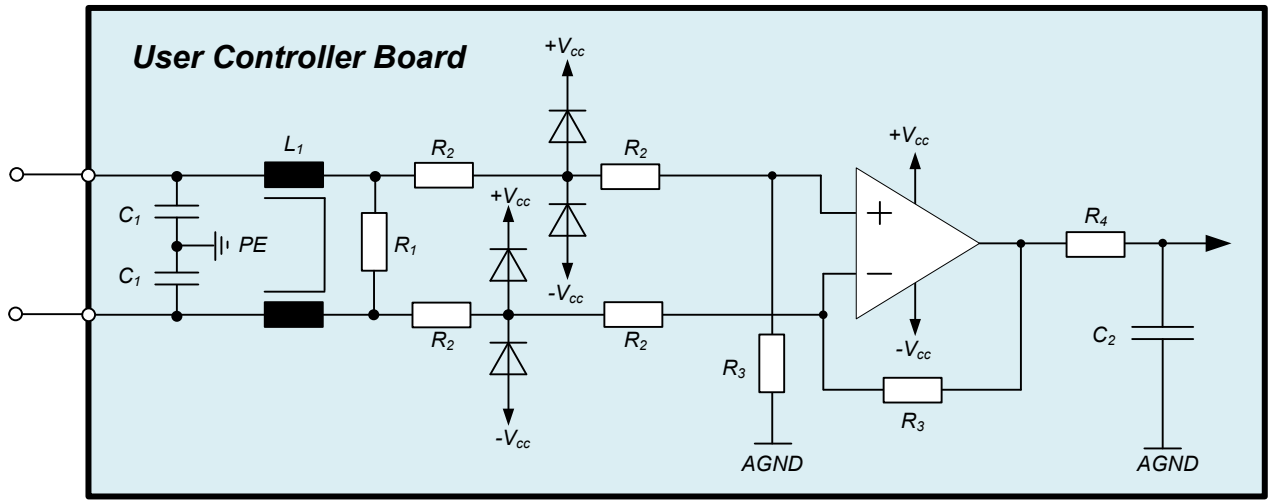
Please ensure that the maximum current driven by the output of the operational amplifier does not exceed 5mA.

A common mode choke and 100pF capacitors are used on the outputs to obtain high noise immunity.

On the user controller board a differential amplifier should be used which is connected to the analogue output and the corresponding ground signals (CMN_TEMP_GND, CMN_DCL_GND, HB_I_GND). This ensures accurate measurement of the analogue signals because there is no voltage drop on the analogue ground wires due to the high input impedance of the differential amplifier (refer to Figure 20).

A description of the equivalent analogue input circuit relevant to the user's controller board is shown in Figure 15.

Figure 15: Application example – symmetric wired differential amplifier. Terminal description HB_I and HB_I_GND for current measurement



The recommended values below have to be checked in the application.

- The equivalent input capacitance should not be higher than 1nF for current measurement and 10nF for temperature and voltage measurement to achieve stable operation of the amplifier circuit on the SKiiP®4 board. Its signal response has to be checked in combination with the used signal cable.
- C1 leaks differential and common mode high-frequency interference currents. This capacitor reduces the bandwidth of the analogue signal. This can lead to control problems like AC current harmonics. Depending on the application PE should be connected to an appropriate ground, e.g. chassis ground.
- Common Mode Choke L1 is used for filtering of common mode currents. The current-compensated ring core choke with ferrite core and rating 51µH/0,5A is recommended.
- Resistor (R1). The interference sensitivity of the overall circuit (user control, driver) is reduced by a continuous current flow through this resistor. Recommended value: 10kOhm

Please note: Capacitors should not be used in parallel to the feedback resistor (R3) and also not to the resistor of the non-inverting input to ground (R3). These capacitors have often high tolerances, so the common-mode rejection of the circuitry is reduced by this effect. No capacitor should be connected between the plus- and the minus-pin of the operational amplifier as well. This additional corner frequency can lead to an oscillating signal.

- The input resistor (R2) should be split and installed between the clamping diodes. The current through the diodes is limited by this resistor. A diode with a low reverse current should be selected e.g. BAV99.
- To achieve a good noise performance a low-impedance feedback resistor should be used (R3). Recommended value: 25kOhm.
- A low pass filtering stage should be implemented to avoid remaining differential interferences. It can be realized by a simple R-C network (R4, C4) at the end of operational amplifier. The corner frequency of the filter should be adjusted to the behaviour of the operational amplifier used and the necessary bandwidth of the analogue signal (Temp/DC-Link/Current).
- A Rail-to-Rail amplifier is recommended for better performance. If not available the OPAMP's negative supply terminal shall be connected –VCC, e.g. to negative voltage instead of ground in order to use the complete voltage range of the amplifier, especially close to 0V. The possible negative output voltage of the amplifier has to be considered when designing the interface circuit.
- AGND should be connected to the ground of the analogue signal processing at the user controller board.

5.2.6 HALT Logic Signal

The HALT signal provides the following characteristics and functionality:

- enabling and disabling the gate driver
- dominant/recessive (settable and readable by driver and user controller board)
- low active (LOW = IGBT driver disabled, HIGH = IGBT driver enabled)
- digital signal referred to the driver supply voltage VS

The driver will set the HALT signal to LOW state:

- during power on reset,
- when an error status is active (refer to chapter 5.3.7).

The driver releases the HALT signal (recessive HIGH state):

- after the power-on reset time has elapsed **and** no error is present **and** both TOP/BOT signals are LOW
- after the error reset time has elapsed **and** no error is present **and** both signal inputs TOP/BOT are LOW

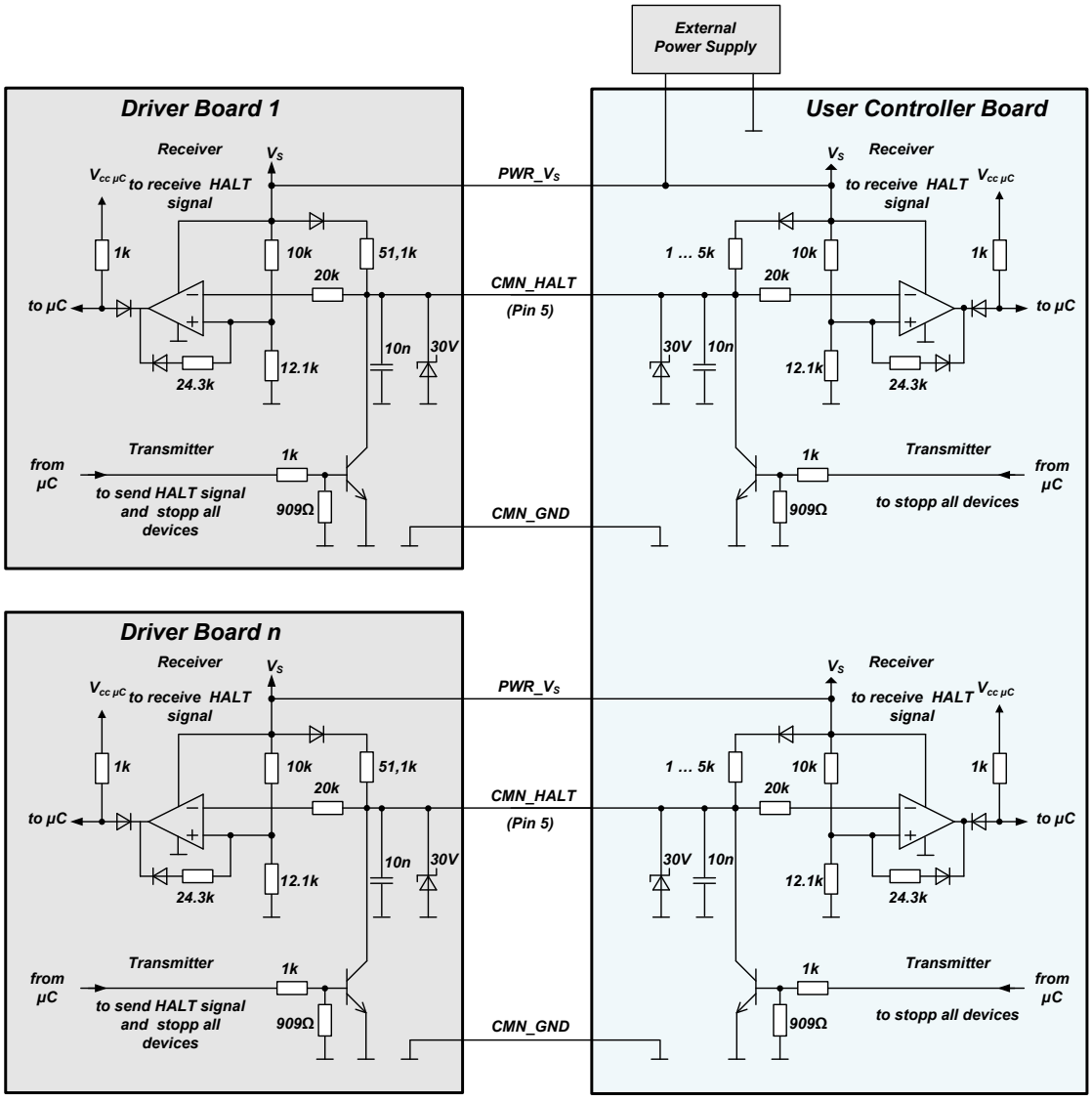
The HALT signals of all SKiiPs in one application can be connected together. Also, other hardware components can be connected to this signal, when an open drain/collector output is implemented. In this case all signals that are connected to the HALT signal are wired-ored. That means the HALT signal is set to LOW state when one of the connected SKiiPs is not ready to operate.

Please note: In this paralleled configuration there is no possibility to see which SKiiP 4 set the HALT signal. For this purpose, the CAN-diagnostic interface should be used

This parallel connection of HALT signals provides a fast disabling of IGBT switching in case of an error or power up. Hence, the operation of such paralleled SKiiP 4 can only start when all SKiiP 4 are ready to operate. The HALT signals of all SKiiPs in the application can be connected to the controller separately, too, as shown in Figure 16. The circuit on the driver board is shown on the left-hand side. The gate driver can be set into HALT state by setting the CMN_HALT signal to GND at the user controller board.

The HALT signal is pulled to GND by an integrated transistor. Pull up resistors are connected on each driver board and on the user controller board. In order to keep the current low when several SKiiP units are connected in parallel the pull up resistor on the driver board is relatively high (51,1kOhm). The pull up resistor on the user controller board should be at least 1kOhm. A delay of the HALT signal due to the capacitors on the driver board (10nF) must be considered.

Figure 16: Application example of the HALT signal processing for separated SKiiP 4 systems



Please note: If the HALT signal is not used it must be connected to the Vs pin according to Figure 23 (not used digital signals).

5.2.7 CMN_GPIO1 signal

The CMN_GPIO1 signal is available at Pin 18 of the SKiFace interface.

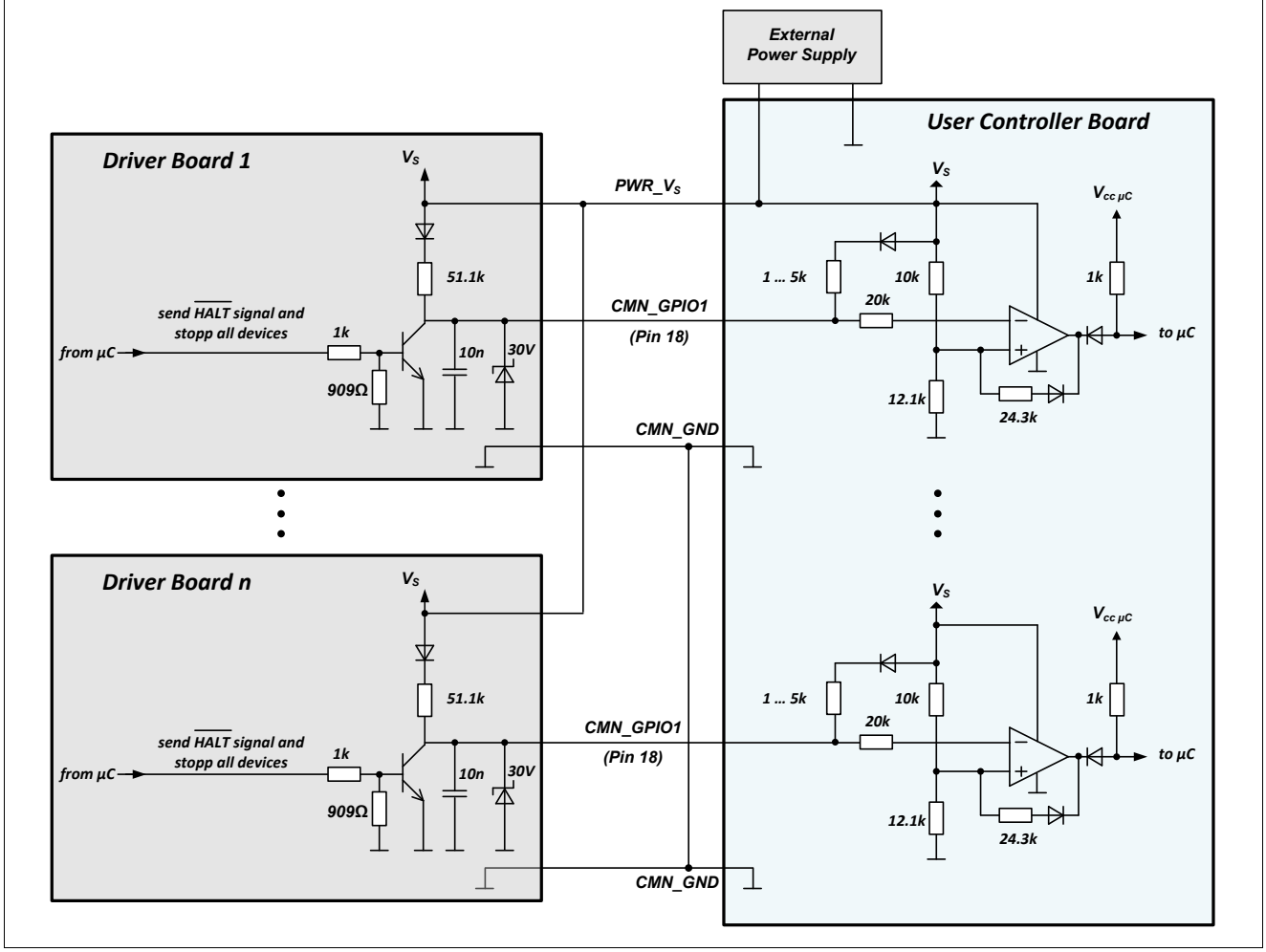
The CMN_GPIO1 signal is the inverted HALT signal ($\overline{HALT}$) that can be used as error output signal of the SKiiP 4 (in case of activated FRT-function please refer to chapter 7.7 for further information).

Please note: As the CMN_GPIO1 signal is the inverted HALT signal, there is no possibility to see which SKiiP 4 has set the error output signal. For this purpose, the CAN-diagnostic interface should be used

Figure 17 indicates:

- on the left-hand side the output stage of the CMN_GPIO1 signal
- on the right-hand side an example of the input stage of the user controller board for each CMN_GPIO1 output of several SKiiP 4

Figure 17: Application example of the CMN_GPIO1 (inverted HALT signal) as error output signal



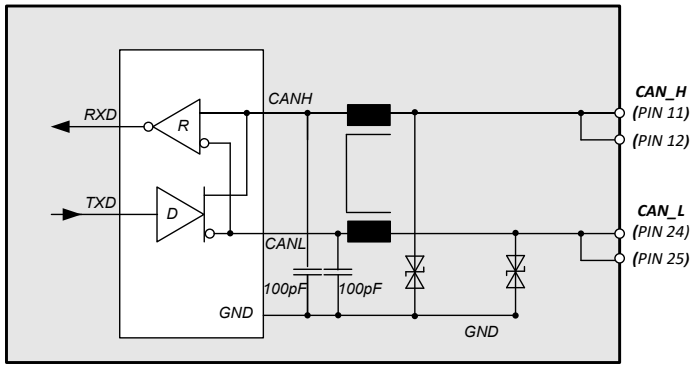
5.2.8 CANbus interface

The CANbus interface employs comprehensive interaction with the SKiiP 4, e.g. it provides the possibility to read out the type of error occurred and when it occurred. In addition to this, the CAN-interface is used to parameterize and configure, e.g. to activate/deactivate dedicated features of the SKiiP 4, and to allow a customization to a certain extent. That configuration through the CAN bus allows protection parameter settings like the DC-link trip function for example as well as the activation of a dedicated function to ride through extraordinary wind turbine specific application conditions. For further details please refer to the FRT-function (see Chapter 7.7) or DC-Link trip level deactivation.

Please note: By deactivating the supervision of V_{DCtrip} the related SKiiP4 data sheet limits must be strictly observed by the user. The violation of these limits can lead to the threat to life or physical condition, as well as to a damage of the SKiiP.

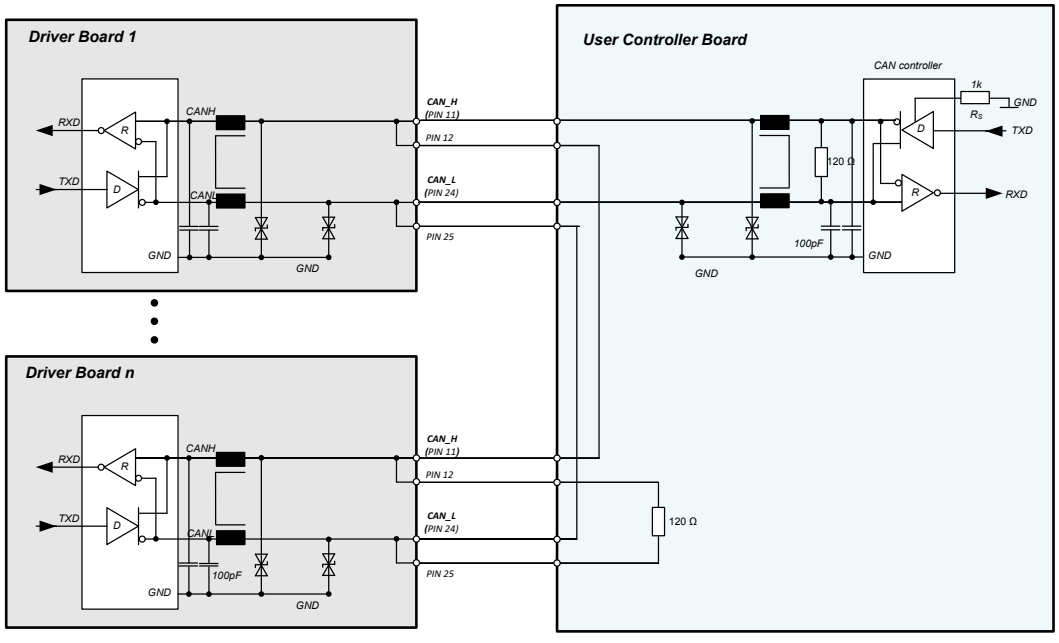
The CAN-Interface is available at Pins 11 and 12 (CAN_H) and at the Pins 24 and 25 (CAN_L) as shown in Figure 18.

Figure 18: CAN-Interface



If several SKiiP 4 units are used: A CAN-application example as shown in Figure 19 is recommended.

Figure 19: CAN – application example for several SKiiP



For a detailed description of the SKiiP 4 CAN interface please refer to the following document:

- Diagnostic Interface SKiiP4 – CANopen User Manual

5.2.9 Ground Connection

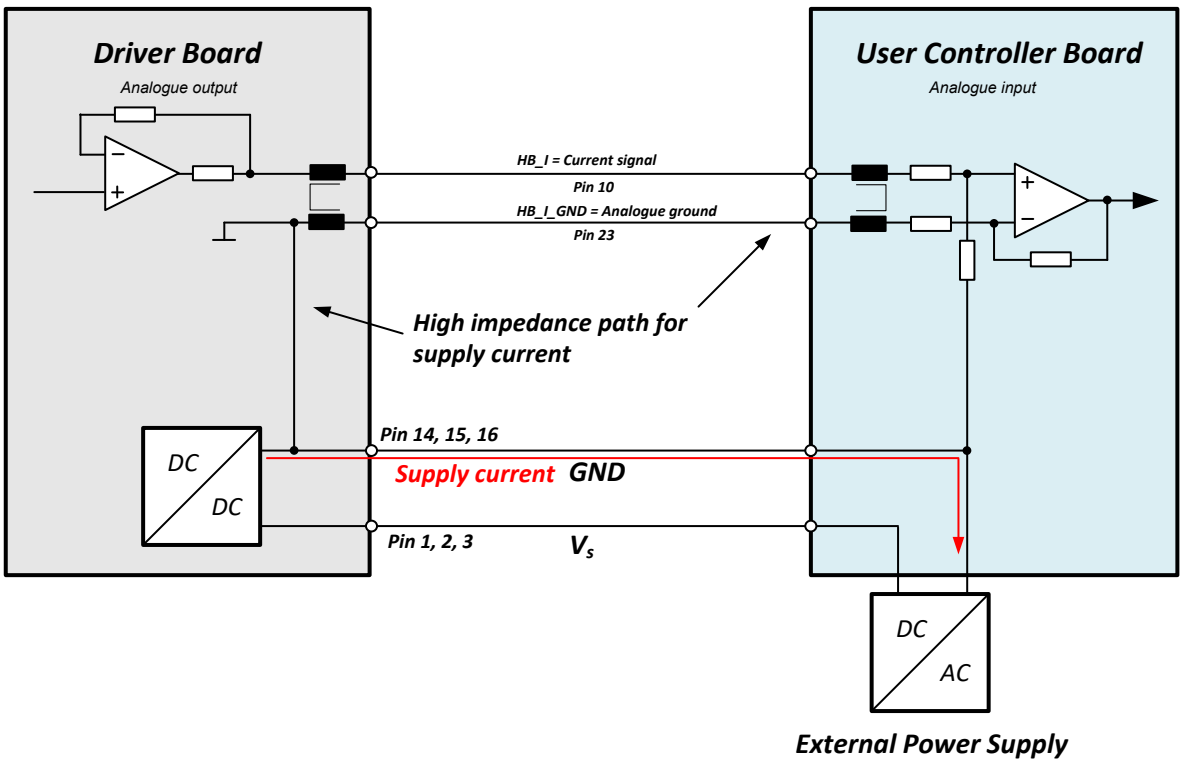
The SKiiP 4 interface has got power grounds, digital grounds and analogue circuit related grounds. The power ground and digital ground are used for as reference for the power supply and as the reference of digital signals, respectively. The analogue ground is used to achieve a more accurate interface of measured analogue signals. All grounds are physically interconnected on the gate driver board. It is allowed to short-circuit all ground potentials except the analogue ground on the user controller board.

The analogue ground should be used as reference to differential amplifier inputs on the controller board to ensure accurate measurement (refer to Figure 20).

Table 9: Ground connections of SKiiP 4

Function	Signal
Power ground and digital grounds	PWR_GND CMN_GND HB_GND
Analog ground	CMN_TEMP_GND CMN_DCL_GND HB_I_GND

Figure 20: Prevention of ground loops by differential amplifier circuitry



5.2.10 Shield and protective earth/chassis connection

The shield of the D-Sub connector is connected to GND at the gate driver board. There is no connection at the gate driver board to heat sink nor to any other protective earth connections. On the user controller board the shield should be connected to the chassis which is linked to Protective Earth (PE) in insulation class 1 systems. This single ended grounding is effective against capacitive coupling e.g. from neighboring conductors since the grounded shield forms the opposite pole of the parasitic capacitance. The interference current flows away via the shield. The GND of the user controller board can be connected to protective earth/chassis either directly or by a suitable capacitor. This connection should be low inductive (e.g. metal bolts from PCB to chassis) and located close to the D-Sub connector. Furthermore, each signal output and input should have a capacitor to chassis. These measures are for bypassing burst signals.

Figure 21: Ground and shield connection. Principle schematics for Ground and shield connection. Principle equivalent circuit of switching signal inputs

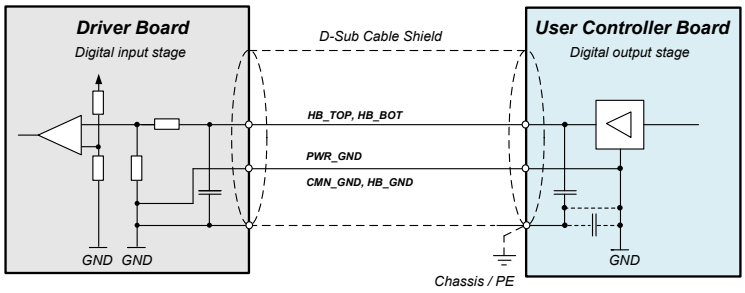
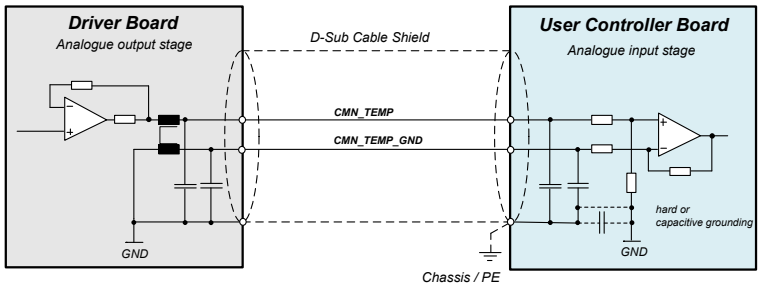


Figure 22: Ground and shield connection. Principle equivalent circuit for analogue output signals (Example: Temperature output)



5.2.11 Reserved or not used signals

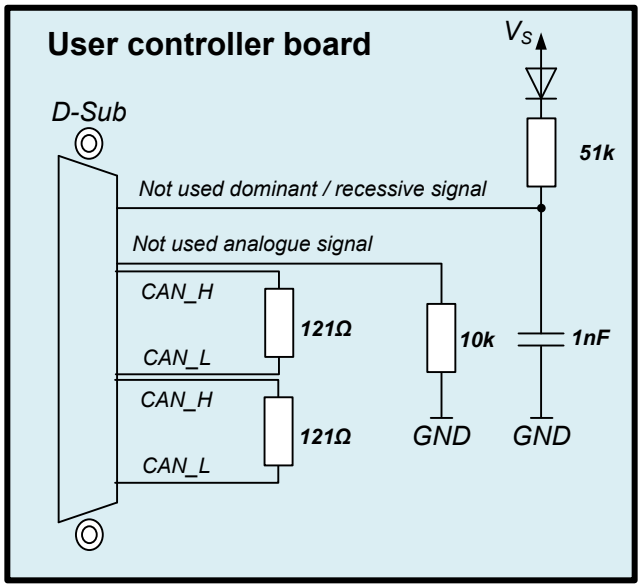
Unused pins of digital signals (CMN_GPIO1, CMN_GPIO2) at the user controller board should be connected to V_S by a 51 kOhm resistor in series to a diode as shown in Figure 23.

The diode prevents from supplying the controller from the driver board when the controller is not supplied. Also a capacitor should be connected to GND to damp burst signals.

For the CAN interface it is recommended to connect the CAN open signals by 121 Ohm resistor, in case the CAN interface will not be used.

Unused analogue signals should be connected to GND by a 10 kOhm resistor.

Figure 23: Connection of reserved and not used signals at the user controller board



5.3 Digital signal transmission

The driver board provides two independent signal channels communicating from low voltage to high voltage side to transfer switching and sensor signals. The signals are transferred by dedicated pulse transformers which are designed according to the standard of reinforced isolation.

This approach ensures:

- Avoidance of temperature and aging effects
- Galvanic Isolation between low (primary) and high voltage (secondary) side inclusive temperature and DC-Link voltage feedback
- High noise immunity

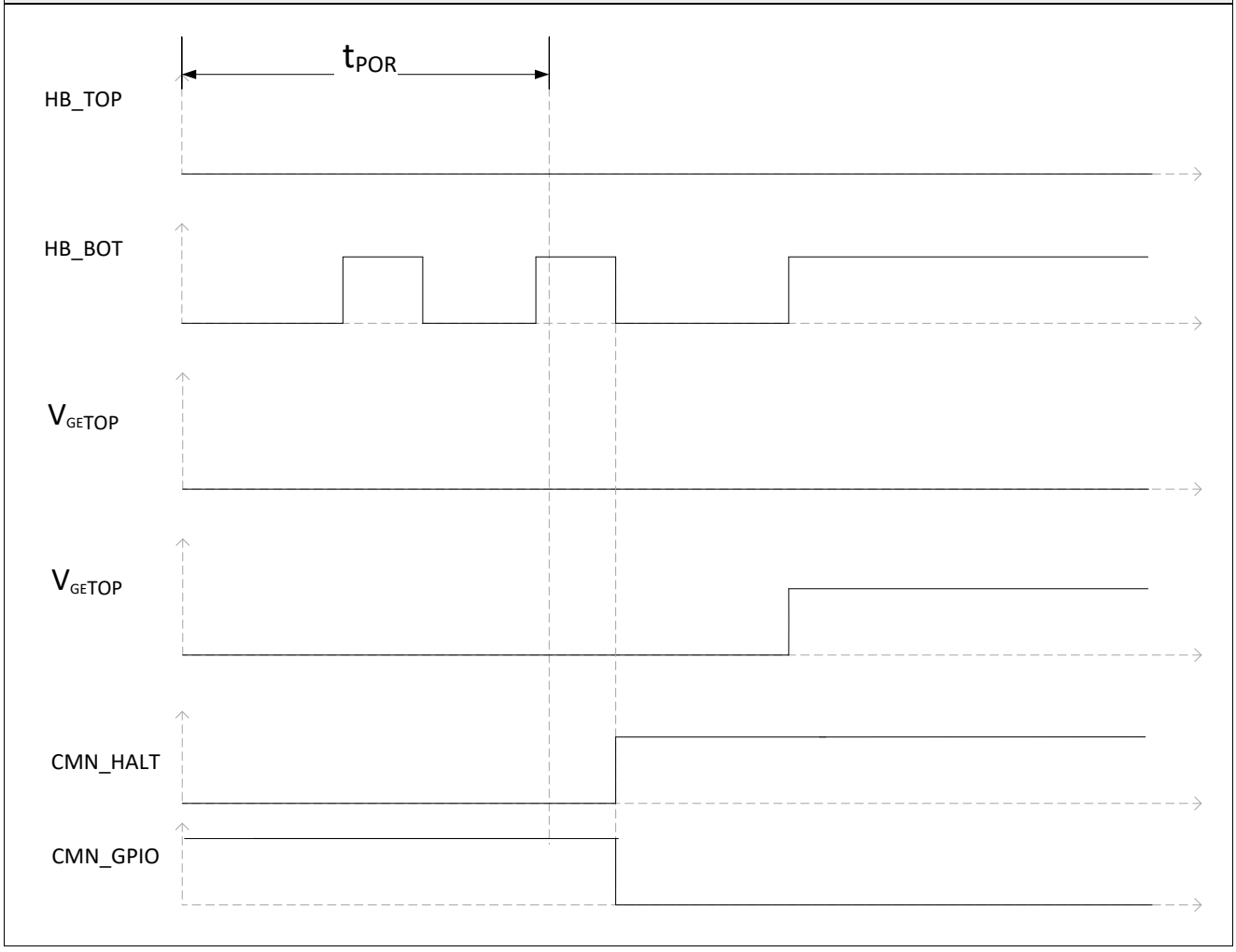
5.4 Power-On-Reset

The Power-On-Reset time is defined as t_{POR} in the SKiiP 4 data sheet.

The driver board processes a Power-On-Reset after turning on the supply voltage. During t_{POR} the HALT signal is set to LOW. Without any error being present, the HALT signal will be released (recessive HIGH-State) after the Power-On-Reset is completed.

Please note: To ensure a high degree of system safety the TOP and BOT signal inputs must be kept in LOW stat during driver's boot up time. After the end of the power on reset, the IGBT operation is permitted. The driver will stay in error mode if switching signals are applied during the boot-up sequence as long as both switching signals are not LOW (see Figure 24).

Figure 24: Power-On-Reset timing diagram



5.5 Interlock Dead Time Generation

The interlock dead time is defined as t_{TD} in the SKiiP 4 data sheet.

The dead time circuit prevents that TOP and BOT IGBT of one half bridge are switched on simultaneously. It is allowed to control the SKiiP 4 by inverted pulses, e.g. without controller generated dead time.

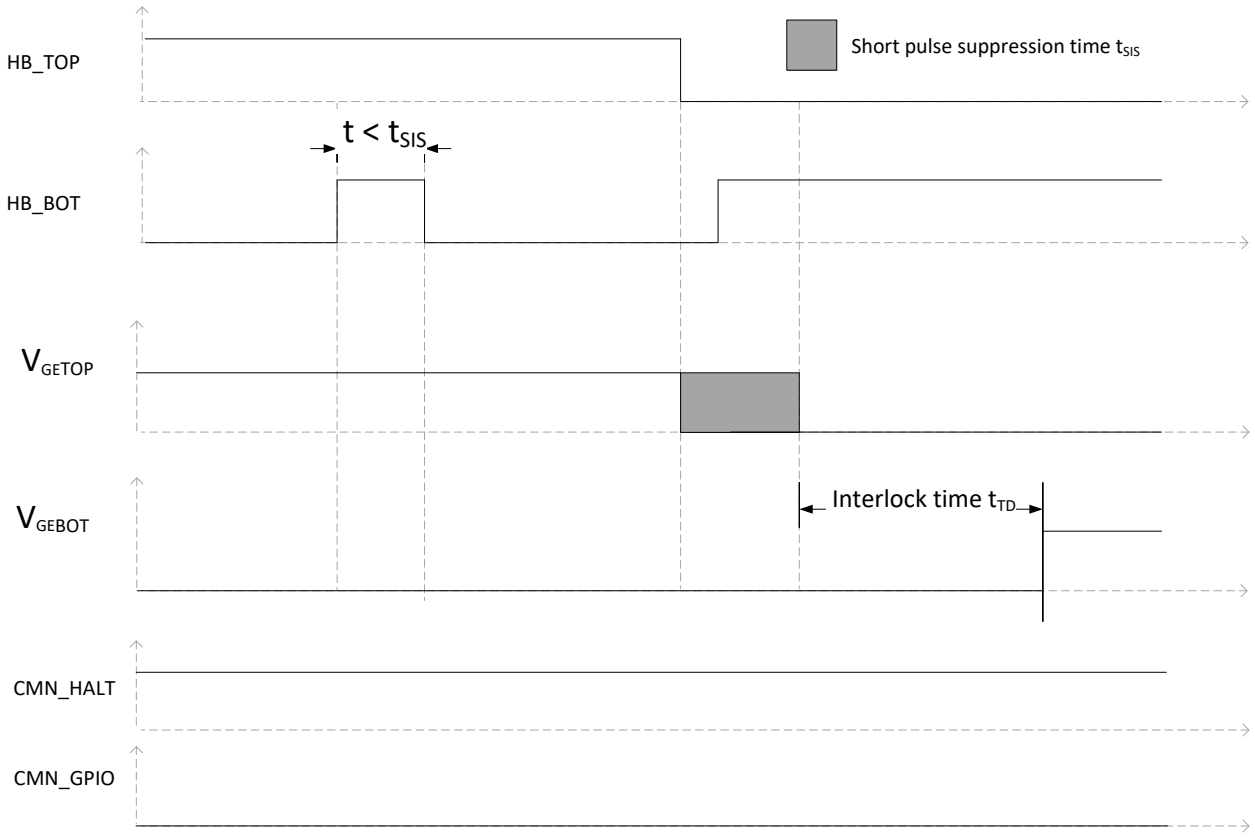
t_{TD} is not added to a dead time provided by the controller (see Figure 25).

5.6 Short pulse suppression

The short pulse suppression time is defined as t_{SIS} in the SKiiP 4 data sheet.

This function suppresses short turn-on and off-pulses at the pins HB_TOP and HB_BOT of the SKiFace interface. In this way the IGBTs are protected against noise which can occur due to burst on the signal lines. If a pulse is shorter than t_{SIS}, it will be suppressed, the other channel will remain on. No error signal will be issued.

Figure 25: Short pulse suppression



5.7 IntelliOff

The SKiiP 4 has two different gate turn-off speeds determined by the internally connected and optimized gate resistors. The suitable gate turn-off speed will be chosen as a function of the actual measured AC current value. As shown in Figure 26, there are two different turn-off speed scenarios:

Figure 26: Turn-off speed scenarios

SKiiP 4 types with integrated IntelliOff function are listed in Table 10.

⊘ = not implemented, ✓ = implemented

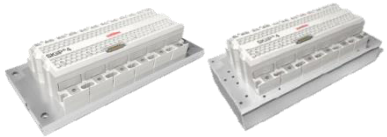
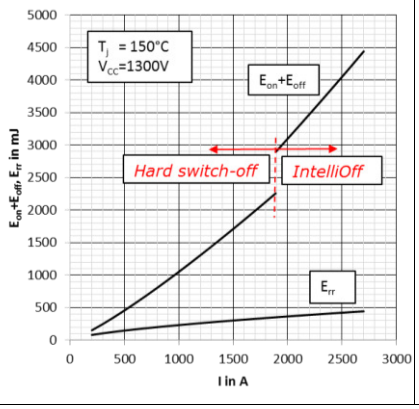
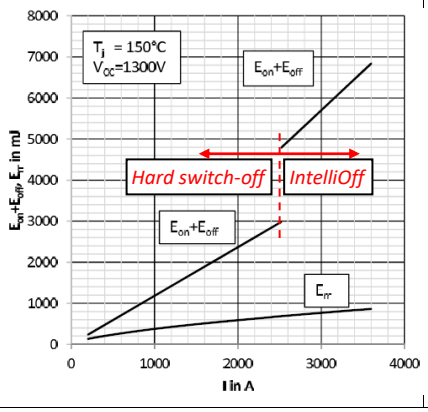
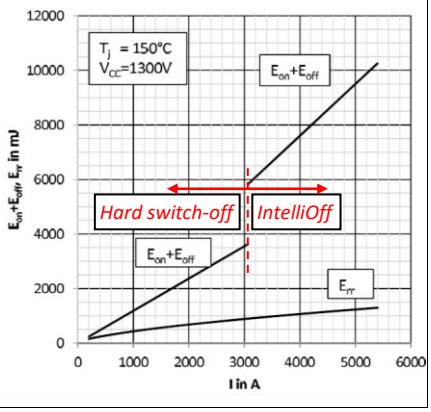
Table 10: IntelliOff functionality

	3GB	4GB	6GB
SKiiP voltage class			
			
SKiiPxxxxGB12 (1200V)	⊘	⊘	⊘
SKiiPxxxxGB17 (1700V)	✓ *	✓	✓

* IntelliOff is only available for 3GB SKiiP 4 with part Nr. 20602xxx

In the IntelliOff mode the IGBT is turned-off by using higher gate resistors compared to normal turn-off.

Table 11: Power loss impact of IntelliOff operation

3GB	4GB	6GB
		
		

Please note: When operating two or more SKiiP 4 modules in parallel connection, the GPIO2 port is used to synchronize the IntelliOff mode for widely balanced current sharing when IntelliOff is activated. The GPIO2 must be assigned to this functionality before by a command through the CAN interface. Then the ports of all parallel operating SKiiP 4 modules have to be connected.

5.8 Error Management

A failure caused by

- Under voltage of the primary side (refer to chapter 5.8.2)
- Exceeding maximum switching frequency (refer to chapter 5.8.3)
- Overlapping of TOP/BOT switching signals (refer to chapter 5.8.4)
- Internal bridge short circuit (refer to chapter 5.8.5)
- Exceeding maximum DCB-sensor/driver temperature
- DC-link overvoltage
- Load overcurrent (OCP)
- Internal driver error

will set the HALT signal to LOW state (indicating that the SKiiP 4 is not ready to operate) as long as the error is present, or at least for the "error memory reset time", t_{pRESET} (refer to SKiiP 4 data sheet, page 2). The IGBTs will be turned-off and switching pulses from the controller won´t be transferred to the output stage. During this time the driver will check if the switching input signals HB_TOP and HB_BOT are set to LOW. If this is the case and no error is present anymore the driver will release the HALT signal. If the input signals have not been switched to LOW state, the driver will pull the HALT signal to LOW (dominate) as long as the switching input signals HB_TOP and HB_BOT are not LOW. So, in case of error the switching input signals HB_TOP and HB_BOT should be set to LOW within the error memory reset time t_{pRESET} and not be activated before the HALT signal is in HIGH state again (see Figure 29).

Please note: The DC-link overvoltage monitoring is disabled at 1500V Photovoltaic SKiiP 4 Systems

5.8.1 Error delay time, $t_{d(err)}$

The error delay time is the propagation delay time of an error. This time is different for the different types of errors. The precise values for each specific error type can are summarized in Table 12.

Table 12: Error delay time

Type of error	Typical values
DC-Link overvoltage	160 µs
Overcurrent protection (OCP-error)	2 µs
Short circuit protection (SCP) by Vcesat monitoring	3 µs
DCB-sensor over-temperature	6 ms*
Exceeding maximum switching frequency	6 µs

*35ms for SKiiP 4 with part nr. 20601xxx

5.8.2 Under Voltage Protection (UVP) supply voltage

The gate drive board is equipped with an under-voltage protection of the supply voltage. The UVP of the primary side monitors the supply voltage V_s. Table 13 indicates the trip level.

Table 13: Signal characteristics of Under Voltage protection of the primary side

Signal Characteristics	Typical values
Undervoltage protection trip level	18.0V
Threshold level to reset after the failure event	18.5V

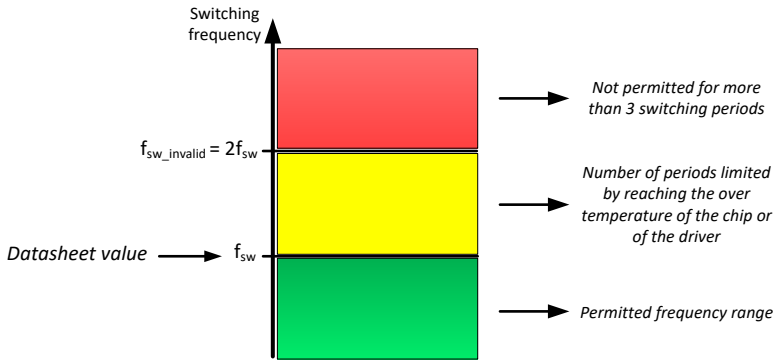
If the supply voltage of the driver board drops below the trip level, the IGBTs will be turned off. The switching input signals HB_TOP and HB_BOT will be ignored, and the status signal HALT is set to LOW state. The system will restart after the error memory reset time t_{pRESET} (refer to SKiiP 4 data sheet, page 2), if the supply voltage exceeds the reset threshold level after the failure reason has disappeared **and** if the switching input signals HB_TOP and HB_BOT are set to LOW.

5.8.3 Exceeding the maximum switching frequency

The maximum switching frequency is defined as f_{sw} in the corresponding SKiiP 4 data sheet.

In order to prevent the module against overheating, the switching signal inputs HB_TOP and HB_BOT are monitored with respect to oscillations. An error latch will be set if the switching frequency is higher than twice the corresponding f_{sw}. Figure 27 illustrates the frequency ranges.

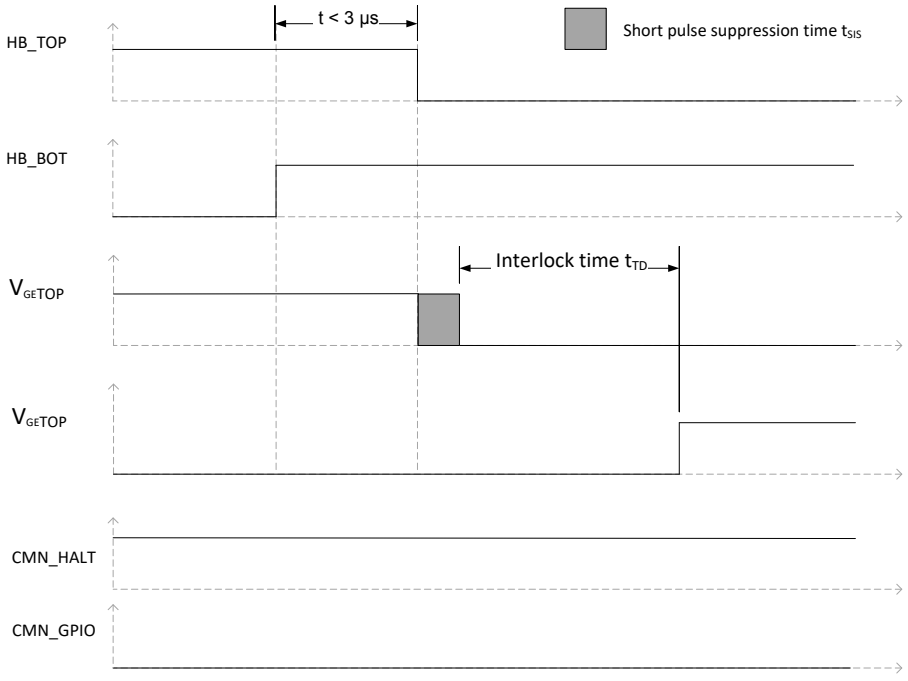
Figure 27: Switching frequency range



5.8.4 Overlapping of switching signals

It is not allowed, that TOP and BOT IGBT of a half bridge are turned-on at the same time. Such an overlapping condition is observed and in case it persists for minimum 3µs the IGBTs are turned-off. After the overlapping situation has ended and the interlock time has elapsed the opposite IGBT will be turned-on. The timing diagram of the error processing in case the overlapping duration is shorter than 3µs, is shown in the Figure 28.

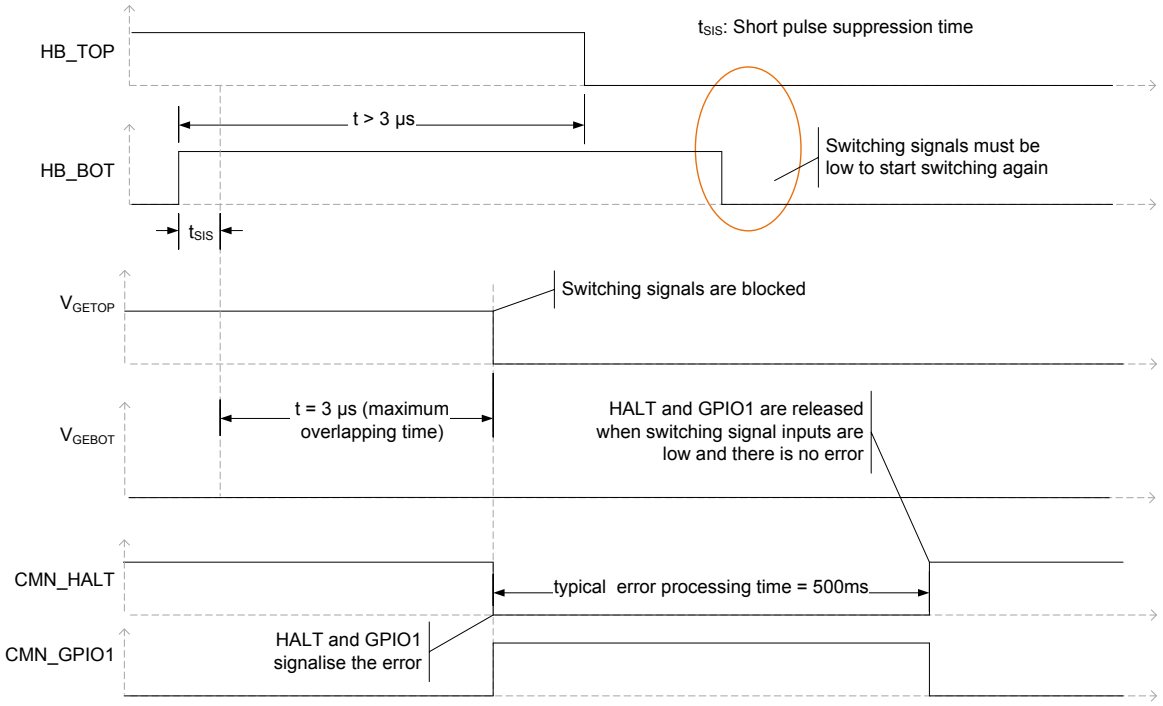
Figure 28: Timing diagram for the TOP/BOT overlapping error processing (t<3µs)



If the overlap time is longer than 3µs both IGBT's will be switched off and the HALT-signal is activated to indicate an error condition. This is shown in the Figure 29.

Please note: Before continuing with the switching operation both switching input signals HB_TOP and HB_BOT must be set to LOW.

Figure 29: Timing diagram for the HB_TOP/HB_BOT overlapping error processing (t>3µs)



5.8.5 Over current Protection (OCP)

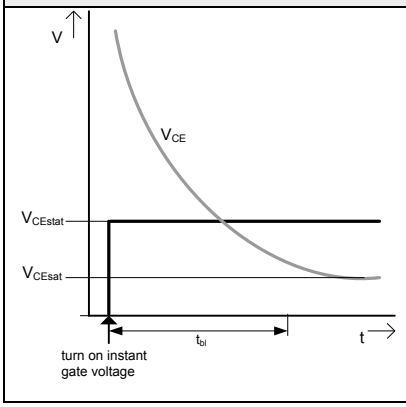
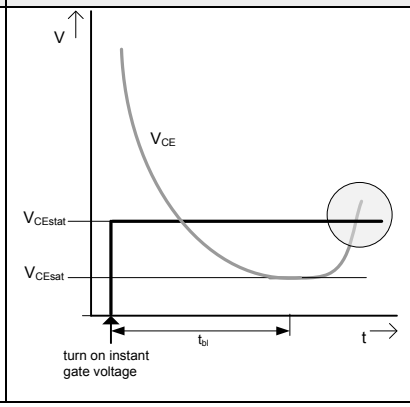
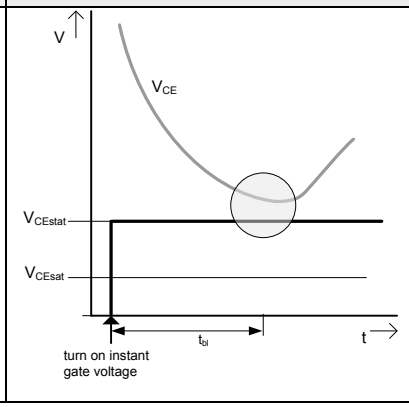
The over current protection (OCP) is a protection that is based on the integrated current sensor measurement and, hence, it protects based on a load imposed current. The application shall be selected to ensure that the peak load current stays safely below the over current protection level. For further details please refer to the corresponding datasheet of the SKiiP 4.

5.8.6 Short Circuit Protection (SCP)

The short circuit protection (SCP) circuit is protecting against short circuit situations by initiating a safe turn-off of the IGBTs. The protection circuit monitors the collector-emitter voltage VCE of the IGBT during the on-state of the device and derives a suitable threshold from this value to turn-off the IGBT in case of a short circuit. Once the threshold level is exceeded the blanking time delay starts and ignores the high current for this period to increase the noise immunity of this circuit. The activated SCP will result in ERROR state and an error signal will be issued correspondingly.

The threshold voltage (V_{CEstat}) and the blanking time (t_{bl}) are listed in the SKiiP 4 data sheet.

Figure 30: Short circuit cases

No short circuit	Short circuit during operation	Short circuit during turn on
		

After the blanking time has expired, the desaturation protection will be triggered as soon as V_{CE} > V_{CEstat} and will lead to a soft turn off of the IGBT (high turn off resistor). The HALT signal will be set to LOW and an error is indicated accordingly.

5.8.7 Thermal protection (over temperature protection)

The SKiiP employs a thermal sensor on the same substrate where also the power chips are assembled. Since the temperature sensor is located close to the IGBT the actual and precise IGBT temperature cannot be acquired from the distance especially not under dynamic load variations. Consequently the protection function derived from the substrate temperature sensor's temperature needs evaluation under the real application conditions such as peak current, load profile etc and suitable protection levels shall be set.

5.9 Analogue signals / sensor functionality

5.9.1 Load current sensor

Each half bridge module (refer to Figure 1) has an integrated load current sensor. The measured current is normalized to a corresponding voltage and available at the SKiFace interface (see Table 7).

Table 14: Signal characteristic of current measurement

Signal Characteristics	Typical values		
	3-fold	4-fold	6-fold
Analogue minimum current trip level I_{TRIPSC} HB_I = 10V	2700 A	3600 A	5400 A
Typical ratio of current analog value [mv/A]	3.70	2.78	1.85
Accuracy of analogue signal @ I_{TRIPSC} over full temperature range	±3%		
Small signal bandwidth, $f0_{Iana}$	50 kHz		

Figure 31: Characteristics between current and the voltage at HB_I, SKiiP 4 3-fold)

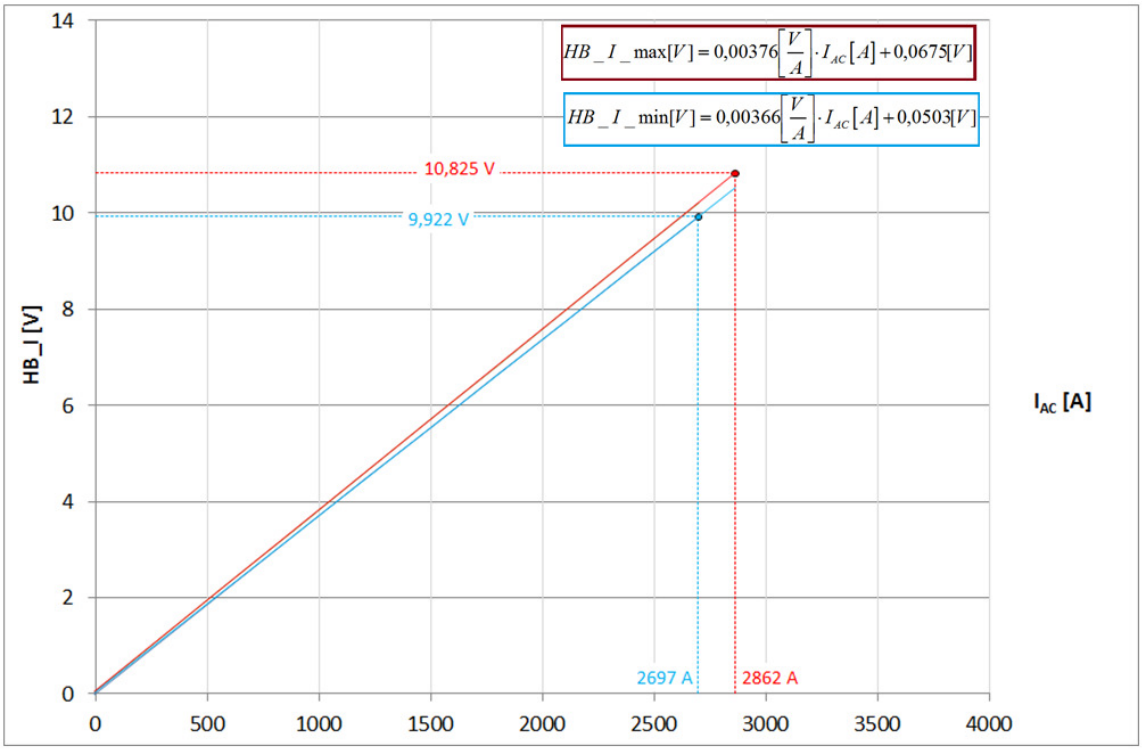


Figure 32: Characteristic between current and the voltage at HB_I, SKiiP 4 4-fold

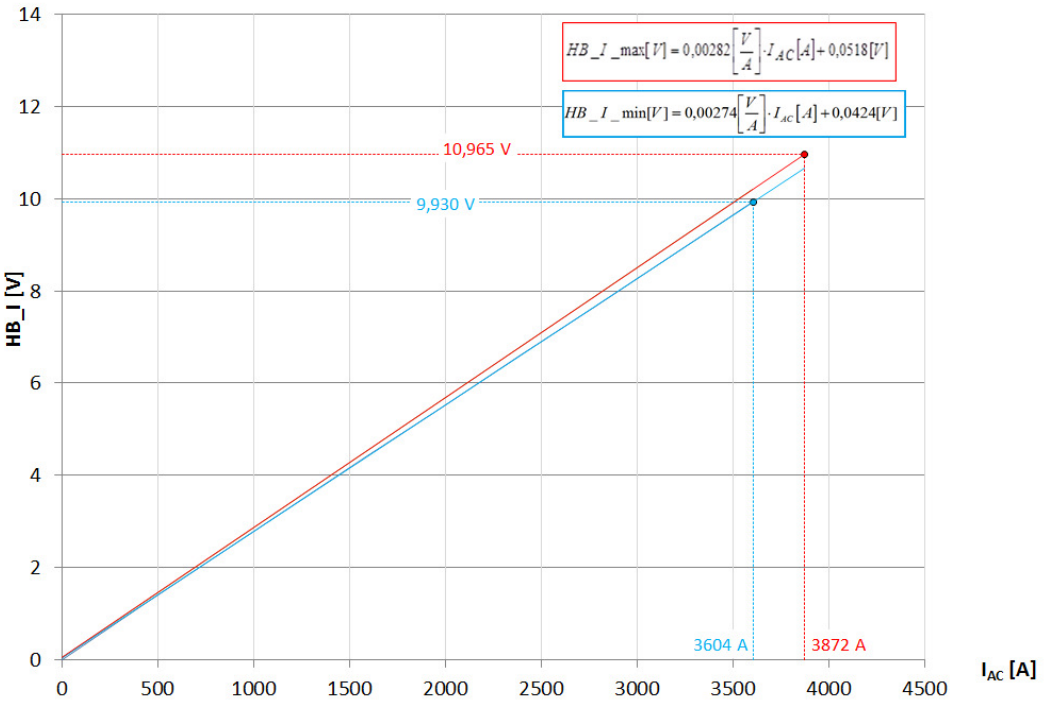
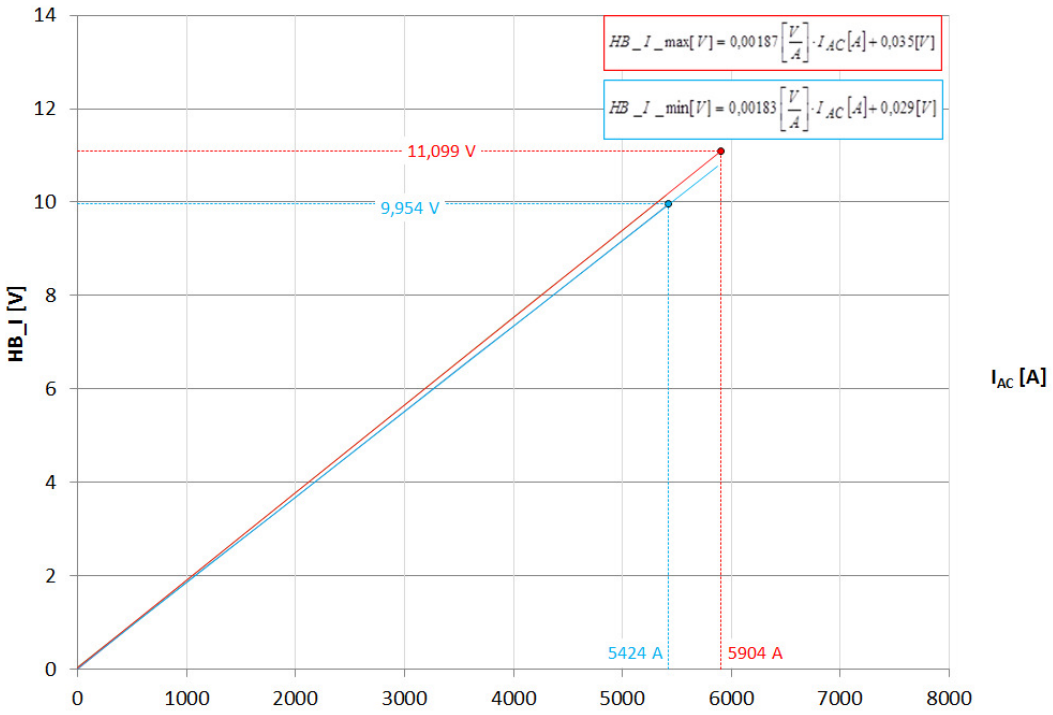
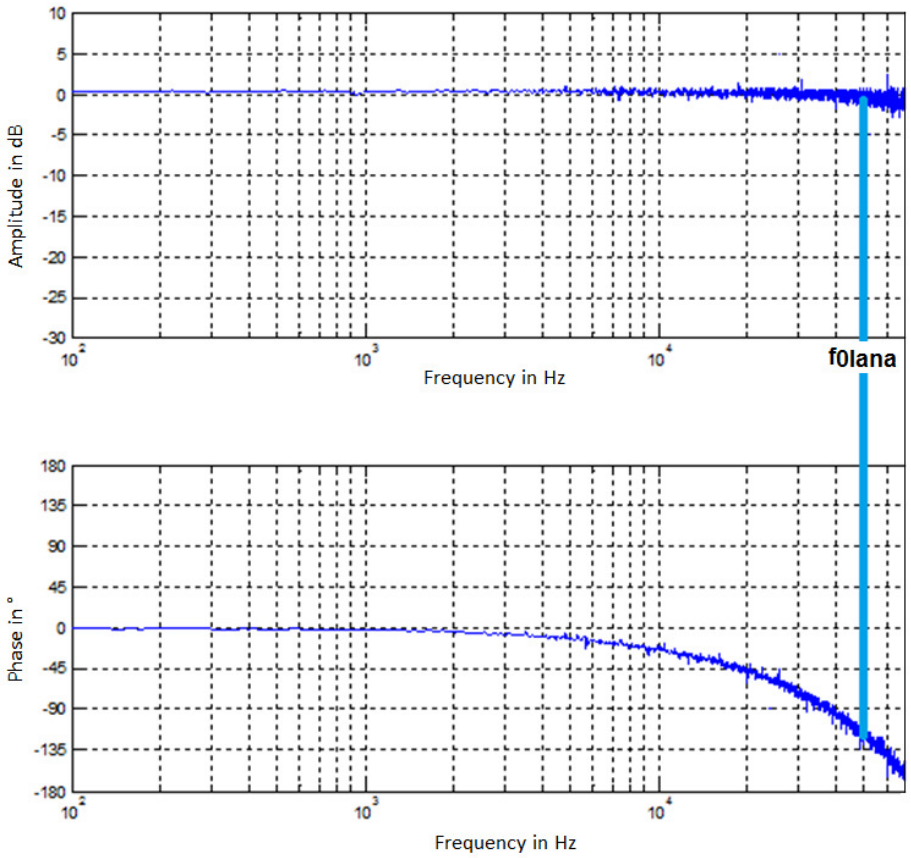


Figure 33: Characteristic between current and the voltage at HB_I, SKiiP 4 6-fold



The value $f0_{Iana}$ given in the Table 14 is marked in Figure 34. At this frequency the amplitude is still not significantly damped.

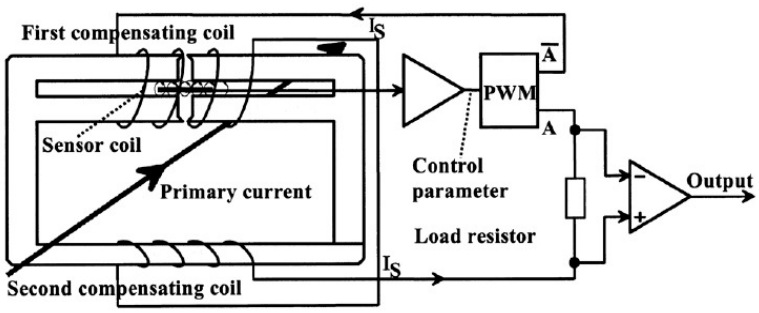
Figure 34: Bode diagram of the AC-current measurement at the SKiiP 4 interface



Current sensor working principle

The current transformers operate using the compensation principle. The magnetic field generated by the load current is detected by a magnetic field sensor. This is a small coil with a high permeable core. Due to the properties of this sensing element there is low gain and linearity failure. An electronic circuit evaluates the value of the field sensor and feeds a current into the compensation coil to keep the effective magnetic field at zero. The demanded compensation current measured by a burden resistor. A measurement circuit generates a voltage that is proportional to the load current. The SKiiP 4 current sensor uses a switch mode controller for the compensation current. Figure 35 illustrates the compensation principle with the current sensor employed in the SKiiP 4.

Figure 35: Compensation principle of SKiiP 4 current sensor



5.9.2 Integrated DCB-temperature sensor

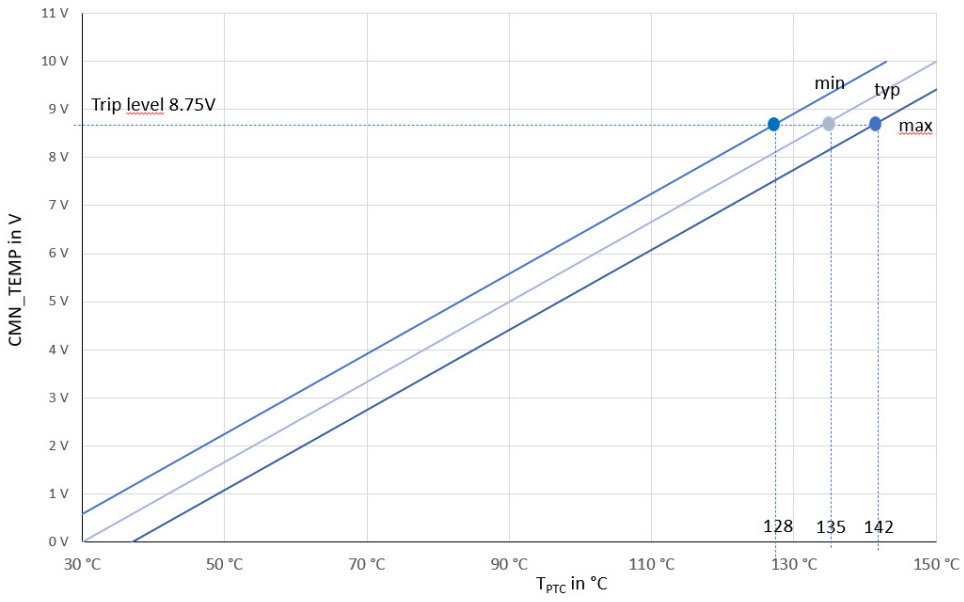
The integrated DCB-temperature sensor is a chip resistor with temperature dependent characteristic. The sensor is placed on the copper trace of the BOT IGBT (collector potential) which ensures that the measured temperature of the DCB is close to the IGBT chip location. The measurement circuit, which is realized on the

secondary side of the driver board, generates an equivalent voltage which is digitized, transmitted to the primary side via a transformer for galvanic isolation and converted into an analogue signal on primary side. The analogue temperature signal is available on the SKiFace interface (see Table 7) with characteristic given below:

Table 15: Characteristics of the DCB-temperature sensor circuit

Temperature signal characteristics	**Value**
Trip level T_{trip}	135°C
Minimum measurable temperature T_{MIN}	+30°C
Analogue temperature signal CMN_TEMP @ 150°C	10V
Analogue temperature signal CMN_TEMP @ 30°C	0V
Accuracy of analogue signal @ T_{trip}	±5%
Bandwidth, f_{0Tana}	5Hz (-3dB)
Threshold level for reset after failure event	90°C

Figure 36: Characteristic between DCB-sensor temperature and the voltage at CMN_TEMP



Please note: the temperature signal characteristic T_{PTC} shown in the Figure 36 is prepared based on the tolerance of the temperature sensor and driver circuit at trip point. The sensor is placed on DBC, so the temperature signal is influenced by thermal stacking of the system and other factors. The impact of these factors is more significant at low temperature area, so that the absolute deviation between several SKiiPs in the same inverter can be up to 14K over the whole temperature range**. For these reasons SKiiP4 temperature sensor is not recommended to be used for control purposes for the temperature range below 100°C.**

In case of over temperature, the HALT signal will be set to LOW and an error is indicated. If the DCB-temperature is lower than 90°C again **and** if the switching input signals HB_TOP and HB_BOT are set to LOW the HALT signal will be released (recessive HIGH state).

5.9.3 DC-Link Voltage Sensing

The DC-link voltage (V_{DC}) is sensed on the secondary side of the driver board between the DC plus and DC minus terminal. After digitizing and transmitting the measured value to the primary side via a galvanic isolation, the digital value is converted back to an analogue signal on the primary side. The analogue DC-link voltage signal is available on the SKiFace interface (see Table 7) with the characteristic given in Table 16.

Table 16: V_{DC} characteristics

V_{DC} signal characteristics	**1200V System**	**1700V System**	**1500V PV**
Analogue DC-link voltage signal CMN_DCL @ 900V_{DC}	9V	6,75V	6,3V
Analogue DC-link voltage signal CMN_DCL @ 1200V_{DC}		9V	8,4V
Voltage ratio	10mV/V	7,5mV/V	7mV/V
Accuracy of analogue signal @ V_{DCTrip} over full temperature range	±3%		
Phase shift, $f0_{Uana}$	1,8kHz		

The characteristic between the DC-Link voltage and the signal on CMN_DCL for 1200V and 1700V SKiiP 4 systems can be found in the Figure 37 and Figure 38 respectively.

Figure 37: DC link voltage sensor output 1200V system

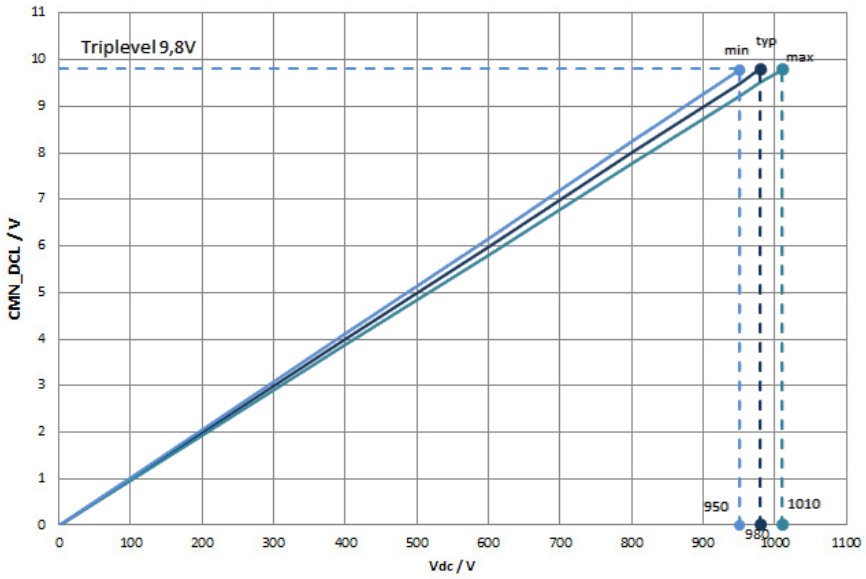
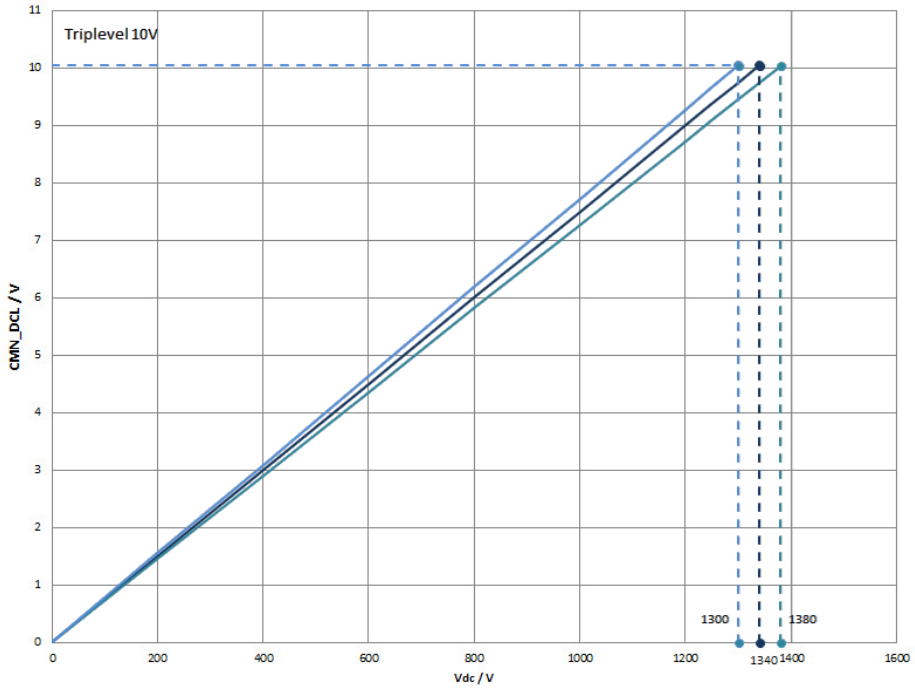


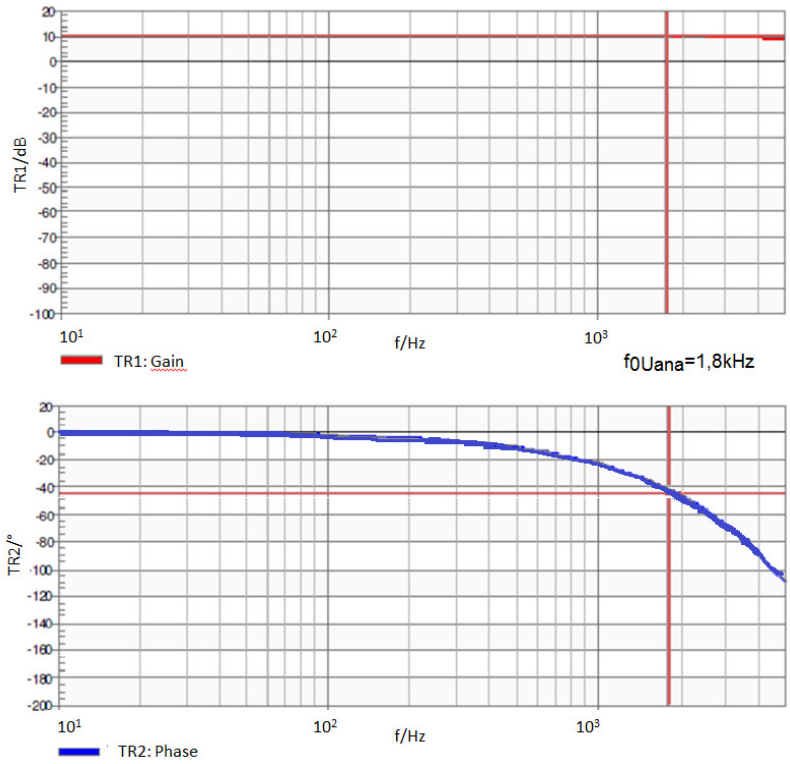
Figure 38: DC-link voltage sensor output 1700V system



The value f_{0Uana} =1,8kHz is marked in Figure 39.

Please note: The SKiiP 4 for 1500V photovoltaic applications do not protect against an DC-link overvoltage. The user must take care of keeping the DC-link voltage within suitable limits in the application.

Figure 39: Bode diagram of the DC-link voltage measurement at the SKiiP 4 interface



6. Power terminals

6.1 Electrical limits

The power terminals have been designed to carry a certain rms current while providing sufficiently low electrical loss. Hence, a feasible rms current level is specified in the corresponding datasheet. Please refer to the corresponding section of the SKiiP module.

6.2 Torque at terminal connections

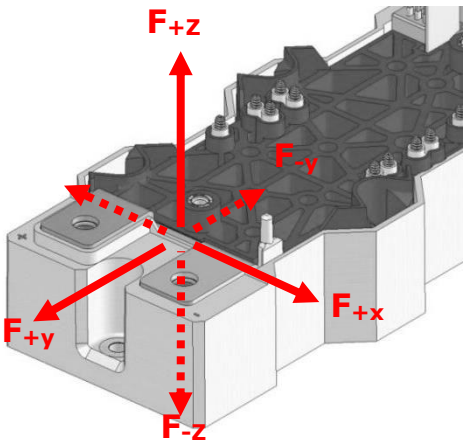
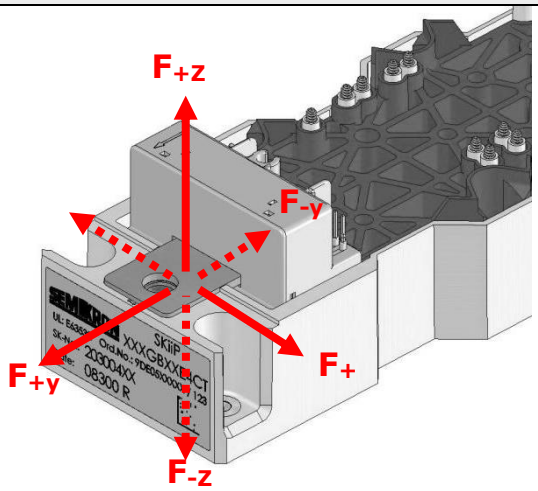
The nuts contained in the plastic housing are utilized to ensure a proper pressure between the external connections and the terminals of the SKiiP. The applied torque to the screws shall be sufficient ensuring such safe connection to the terminals but should not exceed a specified torque to limit the mechanical stress to the plastic housing preventing any damage to the plastic body. Please refer to the corresponding information contained in the datasheet to adjust the mounting tool accordingly.

The power terminals of the SKiiP 4 are widely robust against external forces which may be caused by the connection of the DC-link and load cables. Nevertheless, the SKiiP module is NOT MEANT to support the DC link. The mechanical support must also be provided for the AC connection (e.g. inductor or motor cables) in order to protect the power terminals from mechanical forces and vibration stress. The maximum forces that must not be exceeded are given in Table 17.

Table 17: Maximum allowable forces to terminals

Force	Maximum allowed force [N]
F_{+x}/ F_{-x}	300
F_{+y}/ F_{-y}	300
F_{+z}/	200
F_{-z}	500

Figure 40: Maximum forces at the main terminals

DC-Terminals	AC-Terminal
	

6.3 Mechanical constraints

The following should be considered in the design process:

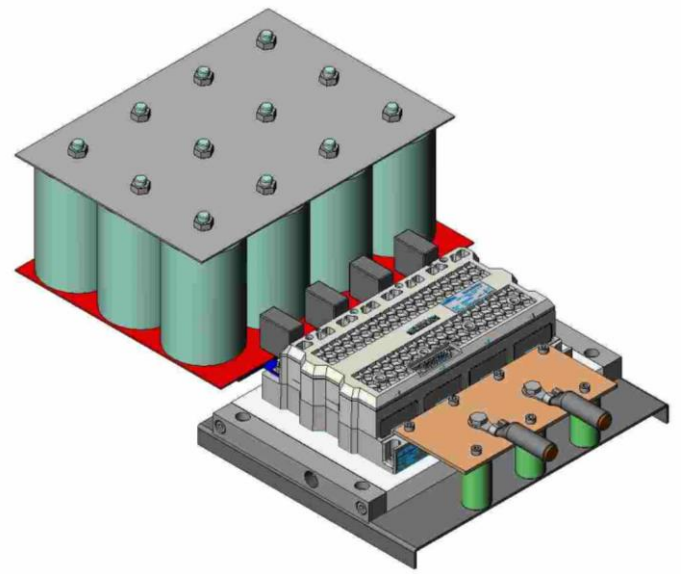
- DC connection:
  - Mechanical tolerances, especially when larger DC-links are used which are connected on more than one SKiiP
- Thermal expansion:
  - The DC-link is heated up under load and expands mechanically. This causes mechanical forces on the terminals.
- Stiffness of terminals for DC connection:
  - The connections should be soft in order to minimize the mechanical forces. This can be realized e.g. by using of tempered copper.
- Terminal hole diameter:
  - Should be large enough that the screw fits through the hole into the SKiiP connection.
- Dimensions of the DC connections:
  - Consider heating and isolation. The terminals must not heat up snubber capacitors.
- Symmetrical layout of DC connection
  - The inductance between the terminals and the DC-link capacitor should be equal for a symmetrical current sharing between the half bridges.

AC connection:

- Symmetrical AC connections for symmetrical current sharing between the paralleled half bridge modules. The load cable should be connected in the middle of the AC terminal and have equal distance to the each half bridge module.
- Connect a plate (e.g. copper) on all AC terminals of one SKiiP
- Cables can be connected on the same plate, but it has to make sure that the cables do not apply force on the terminals (pull or push any direction). Therefore, flexible cables with stress relief should be used.
- The plate should be fixed by fixing poles. These poles shall be mounted directly on to the heat sink or a fixed frame construction and placed close to the SKiiP device.

The design has to be as depicted in Figure 41.

Figure 41: AC connection



Please note: All screws of the AC terminals must be tightened uniformly (not one screw completely fixed before the others) to avoid the warping.

7. Application hints

7.1 Verification of design

Measurements and calculations have to be carried out to be sure that the design works reliably. The following points have to be considered at least:

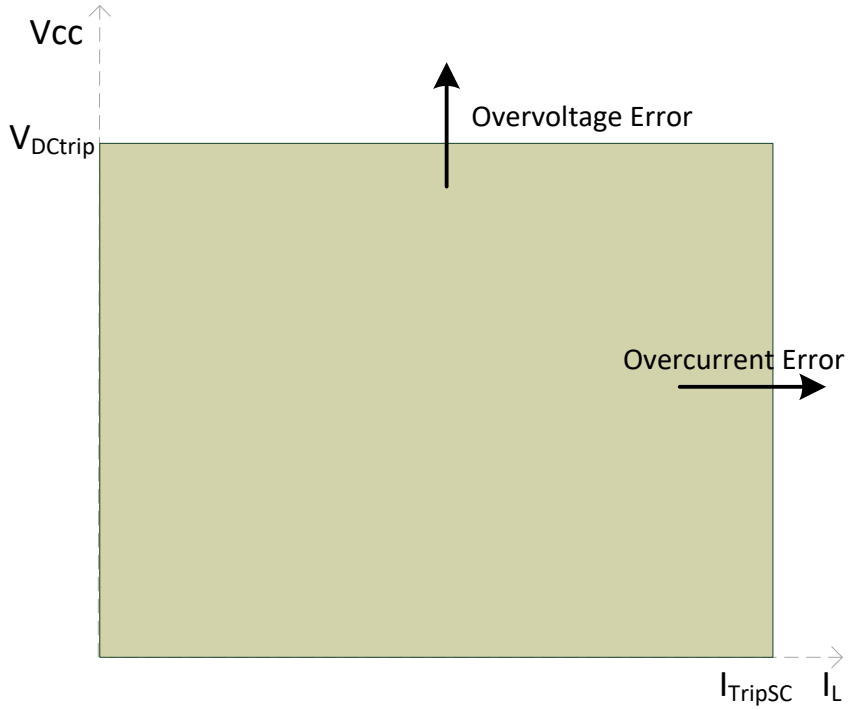
- Maximum blocking voltage V_{CES}/V_{RRM} must not be exceeded in any case (normal conditions, short circuit)
- Ripple current of snubber capacitors
- Current sharing between paralleled half bridge modules
- Recommended IGBT and diode junction temperatures must not be exceeded also considering overload conditions
- Environmental temperatures which affects the lifetime of the electronics
- Load and temperature cycles which affect the lifetime of the power part
- Environmental conditions during operation, transport and storage
- EMC design
- Mechanical design
- Cosmic ray robustness evaluation

Besides these general points application specific conditions and requirements may be considered too.

7.2 Safe Operating Area for SKiiP 4

The principle Safe Operating Area (SOA) for different SKiiP 4 systems is shown in the Figure 42. Please refer to the corresponding data sheets for V_{DCtrip} and I_{TripSC} values for concrete SKiiP 4 types.

Figure 42: Safe Operating Area for standard SKiiP 4



Please note: The curves for Safe Operating Area (SOA) of 1500V photovoltaic SKiiP 4 Systems are shown in the relevant data sheet and differ from this SOA.

7.3 Maximum blocking voltage and snubber capacitors

The maximum blocking voltage V_{CES}/V_{RRM} which is given in the SKiiP 4 datasheet must not be exceeded. It must also be considered that the IGBT switches faster when the junction temperature is low. Suitable countermeasures are low inductive DC-link designs to keep the overvoltage at the semiconductors low among others like the application of snubber capacitors, which should be mounted directly on the DC-link terminals of each half bridge module. The application note AN-7006 "Peak voltage measurement and snubber capacitor specification" provides information how to perform tests in practice and to select the snubber capacitors. The following snubber capacitors have been designed for SKiiP 4. But nevertheless it has to be validated by testing that the capacitors are compatible with the design and that they will not be overloaded.

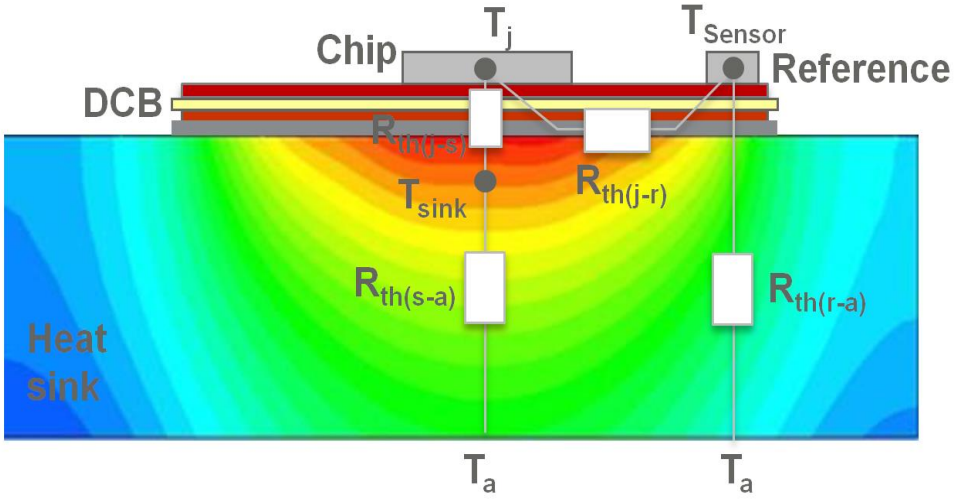
Table 18: Snubber capacitors for SKiiP 4

Capacitance / DC voltage	For use with
680 nF / 1000V	1200V device
330 nF / 1600V	1700V device

7.4 Definition of Thermal Resistance

The definition of the thermal resistances given in the SKiiP 4 datasheet are shown in the Figure 43

Figure 43: Definition of thermal resistances



T_j junction temperature of the hottest chip
T_{sensor} DCB-sensor temperature
T^{sink} heat sink temperature in a drill hole 2mm underneath the chip
T_a ambient temperature (coolant air or liquid)
$R_{th}(j\text{-}r)$ thermal resistance between junction and reference
$R_{th}(j\text{-}s)$ thermal resistance between junction and heat sink
$R_{th}(s\text{-}a)$ thermal resistance between heat sink and ambient
$R_{th}(r\text{-}a)$ thermal resistance between reference and ambient
P_{losses} Power losses of the chip

In general, the thermal resistance between two points 1 and 2 is defined according to following equation:

$$R_{th(1-2)} = \frac{\Delta T}{P_{losses}} = \frac{T_1 - T_2}{P_{losses}}$$

The data sheet values for the thermal resistance are based on measured values. The point of the temperature measurement has a major influence on the thermal resistance because of a temperature profile between the different chip positions and across the heatsink surface.

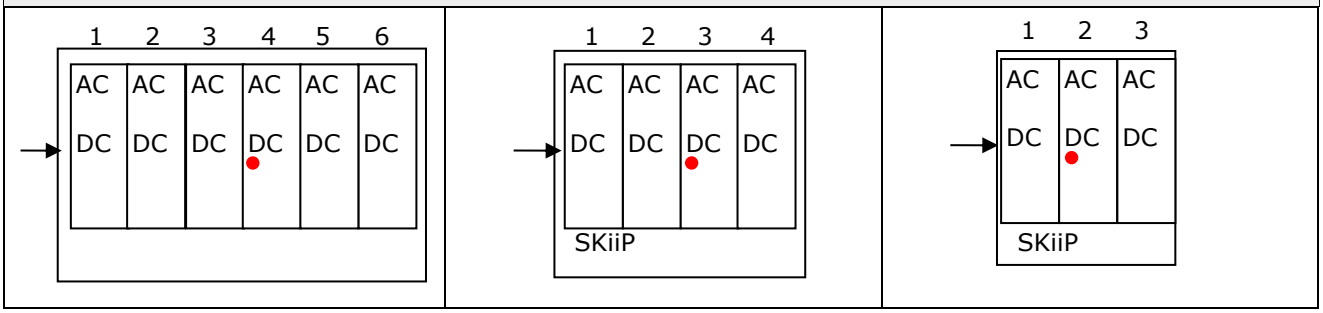
The reference points for SKiiP 4 systems are: virtual junction temperature of the hottest chip (T_j); heat sink temperature underneath the hottest chip (T_{sink}) and DCB-sensor temperature (T_{sensor}). A principal sketch with the positions is shown in Figure 42. The values for $R_{th(j-s)}$, $R_{th(s-a)}$ and $R_{th(j-r)}$ are calculated from these temperatures. SKiiP modules have no base plate, therefore the case temperature T_C cannot be measured without disturbance of the thermal system and the thermal resistance $R_{th(j-c)}$ cannot be given. T_{Sink} is measured in a drill hole 2 mm underneath the heatsink surface. The 2 mm distance guaranties a low disturbance of the thermal path and a minimum effect of heat sink parameters like size, thermal conductivity, cooling medium, etc.

The temperature sensor is located between IGBT and diode chips on the same DBC copper layer at high voltage potential. This ensures an excellent thermal coupling between both power semiconductors and sensor and furthermore a short reaction time on changes in power dissipation.

Only one of the temperature sensors is monitored by the Gate driver. The monitored sensor is in the middle of the SKiiP (refer to Figure 44). The protection level is matched to the maximum operation temperature of the power semiconductors. Since the temperature sensor is close to the IGBT and mounted on the substrate the actual and precise IGBT temperature cannot be acquired. Consequently, the protection function derived from the substrate temperature sensor's temperature needs evaluation under the real application conditions such as peak current, load profile, etc.

During operation there will be a temperature profile along the heatsink from cool at the inlet of the coolant to warm at the outlet.

Figure 44: Sensor position in SKiiP 4 GB (6fold, 4fold, 3fold) with proposed cooling (water inlet) direction



SKiiP 4 are equipped with a variety of heatsinks, some of them are high performance heat sinks. The data sheets contain transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature T_j if the generated losses are known. The thermal resistances given in the data sheets represent worst case values.

Evaluation of thermal impedance:

- Junction to sensor
  $Z_{th(j-r)} = \Sigma R_{th(j-r)n} * (1-e^{-t/Tn})$, n=1,2,3,….
- Sink to ambient
  $Z_{th(s-a)} = \Sigma R_{th(s-a)n} * (1-e^{-t/Tn})$, n=1,2,3,….

Please note: The values for transient thermal impedance given in the data sheets ($Z_{th(j-r)}$) are only valid together with the Semikron Danfoss standard heat sinks and under conditions given in the data sheets. The usage of these values for other heat sinks/conditions might cause deviations in calculation of thermal resistance!

7.5 Cooling and coolant circuit

7.5.1 Prerequisites

The cooling system must be a sealed closed loop system. All items in contact with the fluid and / or used for water connections must be checked for their compatibility with the specified materials used in the SKiiP water cooler and its side parts. Furthermore, the compatibility of the used fluid coolant anti-freeze / inhibitors shall be carefully selected and the producer's conditions and application hints cooling fluid / inhibitor shall be observed strictly to ensure a long lifetime of the cooler. To ensure a defined composition of the resulting cooling fluid preferably distilled water shall be used as base and a suitable amount of the anti-freeze coolant and the suitable amount of inhibitor shall be added. In general water with (German) hardness of 8° or more is not suitable. The pH of the utilized water shall be in a range of 7.0 to 8.5 and a maximum conductivity of 500 µS/cm. The utilized water shall be ideally free from (solved) minerals and ion load to prevent from premature ageing. Further details are available e.g. at the DECHEMA e.V. Corrosion Handbook or any other qualified source of knowledge.

7.5.2 Materials used and fluid composition

The cooling circuit (heat sink) of the water cooled SKiiP 4 IPM consists of two side parts (with inlet and outlet for coolant marked on the corresponding data sheet) and the cooling channels inside the SKiiP cooling plate as well as turbulators for the standard water cooler. The High Performance Cooler (HPC) does not require turbulators. The heat sink cooling channels of each half-bridge of the internal IGBT power module are connected in serial for the standard water cooler and they are in parallel for the High Performance Cooler (HPC). The cooling circuit contains following parts as shown in the table below:

Part of cooling circuit	**Used material**
heat sink plate	EN AW-6060 T66 (AlMgSi 0,5 F22) if nothing else is specified
side parts	EN AW-6060 T66 (AlMgSi 0,5 F22) if nothing else is specified
sealing gasket	EPDM 70 Shore A
turbulators (standard water cooler)	EN 1.4310 (X10CrNi18-8)
heat sink plate with integrated side parts	EN AW 5083 H111

Semikron Danfoss requires the usage of a mixture of water and glycol with corrosion inhibitor in the customer applications. The percentage of glycol in the cooling medium shall be at least 10%.

Please note: The percentage of inhibitor may decrease over the time due to physical processes running in the heat sink during operation, therefore to prevent corrosion for the lifetime of the product the customer is responsible for checking the inhibitor content in the cooling liquid regularly.

All thermal performance data given in the corresponding SKiiP 4 data sheets assume a mixture of 50% water and 50% glycol if not otherwise specified.

Please observe the maximum cooling medium temperature given in the datasheet.

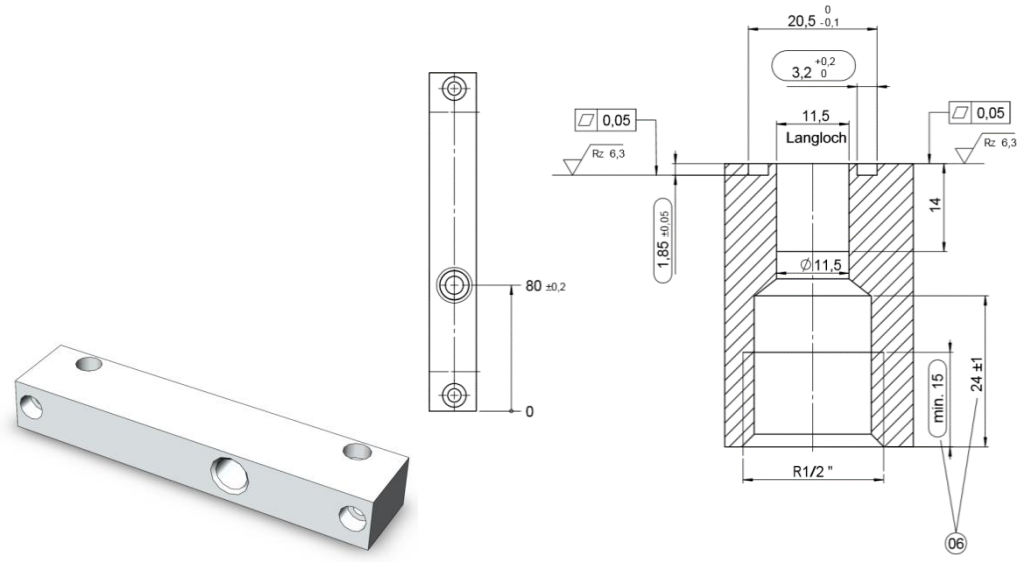
For latest information and hints concerning cooling circuit / coolant please refer to Semikron Danfoss Application manual for Power Semiconductors[2].

7.5.3 Water connection description of water-cooled SKiiP 4

SKiiP 4 side cap:

- Thread R ½ (DIN 259) → correspond to G ½ (DIN EN ISO 228)
- Thread depth 15mm!

Figure 45: SKiiP 4 side cap mechanical drawing



Thread in side cap:

- Older drawings (before 2013) R ½ (DIN 259)
- Newer drawings (since 2013) G ½ (DIN EN ISO 228)

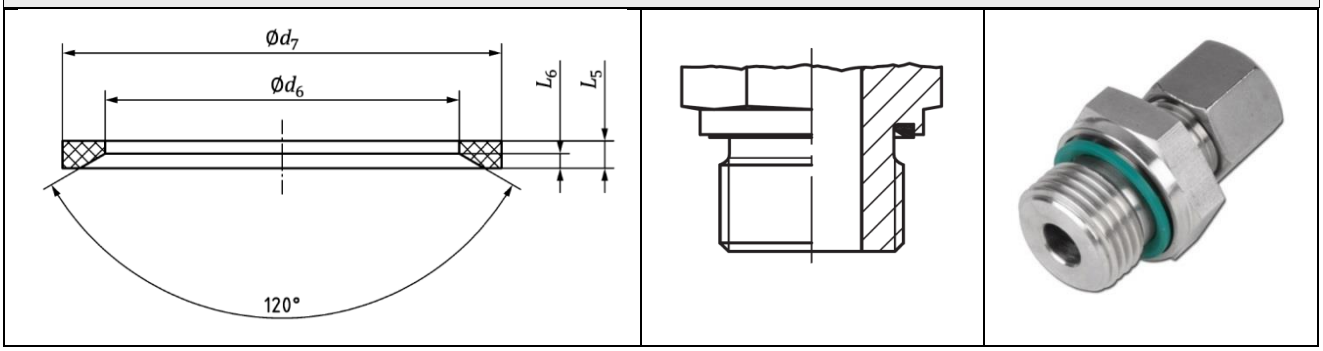
Recommended pipe fitting:

- Fitting ISO 1179-2 — G 1/2 A — L
- Fitting ISO 1179-3 — G 1/2 A — G

Fitting ISO 1179-2 — G 1/2 A — L

- Fitting of shape E according to ISO 1179-2 with G ½ thread, tolerance class A (DIN EN ISO 228), L is for "lower" pressures (max. 250 bar)
- Sealing with a additional profile-sealing ring (rubber) according to ISO 1179-2 – G 1/2 A
- Dimension of profile-sealing ring according to ISO 1179-2:
  - D6 [mm]= 18.5
  - d7 [mm]= 23.9
  - L5 [mm]= 1.5
  - L6 [mm]= 0.8

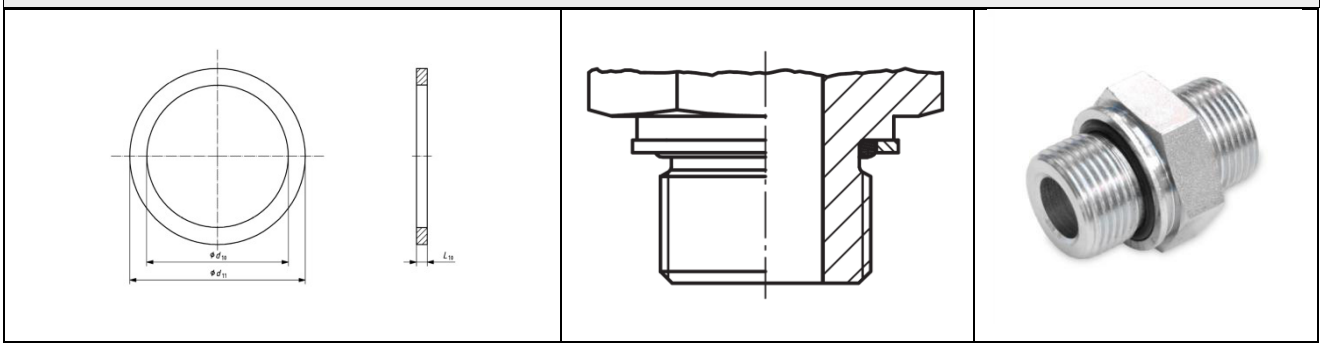
Figure 46: Description of fitting ISO 1179-2 — G 1/2 A — L



Fitting ISO 1179-3 — G 1/2 A — G

- Fitting of shape G according to ISO 1179-3 with G ½ thread, tolerance class A (DIN EN ISO 228), G is the type of the sealing
- Sealing (type G) with a additional O-ring, which is framed by a metal support ring
- Dimensions of metal support ring and O-Ring according to ISO 1179-3:
  - Stützring [mm]: d10 =23.3 | d11 = 28.5 | L10 = 1.9
  - O-Ring [mm]: d8 = 17.86 | d9 = 2.62

Figure 47: Description of fitting ISO 1179-3 — G 1/2 A — G



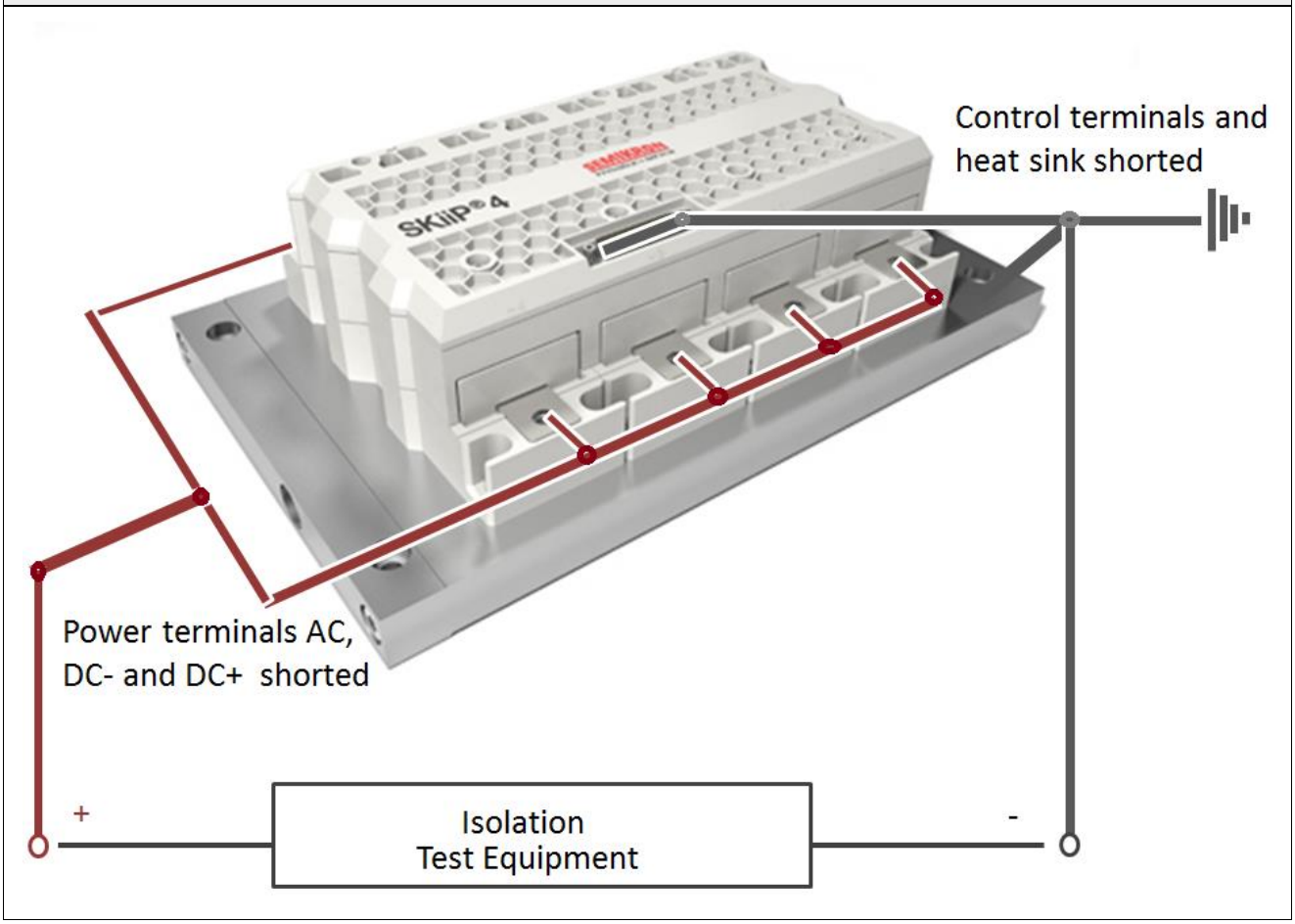
Fitting according to DIN 3852-2 — C — R ½ is not recommended → only for exceptional cases!

Please note: The given specifications for gaskets of the pipe fittings are recommended values and have to be validated by customer depending on production equipment and application.

7.6 Isolation voltage test (IVT)

During production test the isolation voltage of 5600V_{DC} (1700V devices) or 4300V_{DC} (1200V devices), each polarity, is applied to 100% of SKiiP-systems for 1s with a test set up as indicated in Figure 48. These values are also available in the corresponding datasheets.

Figure 48: Graphic presentation of the electrical connections by the IVT procedure



The polarity change (with heat sink always grounded) is only possible when the customer uses a galvanically isolated test control device. Otherwise, the plus and minus pole of the isolation test control device will be shorted.

Please note: Because of the safety measures during and after the test procedure the heat sink should be grounded: When a DUT fails with an arc and this is recognized by the test equipment the DUT typically would be disconnected. However, the DUT might be still electrically charged. In this case it would be dangerous to touch the DUT after the test procedure. In addition to this without grounding the test voltage could drift and the voltage to ground will be even higher than the nominal test voltage.

All isolation voltage tests must be performed at an ambient temperature of 15…35 °C, a relative humidity of 45…75% and an atmospheric pressure of 860…1060 hPa. The standards do not define a certain leakage current value and, thus, the isolation test (dielectric test) is considered passed if no electrical breakdown has occurred, i.e. small leakage currents that might occur are not relevant.

There are two types of an isolation damage:

- Complete breakdown (according to the standards)
- High leakage current (not according to the standards!)

According to the corresponding standards it is required to do an IVT with AC voltage. In contrast to the AC-voltage based IVT a test with DC voltage is recommended because in case of AC IVT the high leakage currents hardly help in the identification of the isolation problem root cause.

It is recommended to ramp up the isolation voltage with 10 kV/s. Faster ramp up leads to capacitive leakage currents and could cause an erroneous activation of the isolation test control unit. A slower ramp up leads to a longer testing time. The start of the test time 1s as specified in the data sheet begins when a ramp up of the full isolation voltage is reached. The isolation voltage could be switched off without a ramp down. After finishing the test, it must be checked that the DUT is not charged anymore.

Please note: The isolation test voltage should not be higher than necessary for the application and stipulated in the corresponding standards.

The isolation measurement is performed in two steps:

- high voltage isolation test
- repeated isolation test

The high-voltage isolation test and repeated test of an isolation barrier can degrade the isolation capability due to partial discharge. During the IVT since the isolation voltage is applied the partial discharge starts after the voltage goes beyond the partial discharge inception voltage. The higher and the longer the voltage stress is applied, the stronger the damage of the isolation through the partial discharge will be. Thus, each IVT leads to a potential weakening of the isolation. Partial discharge in the DCB doesn't necessarily lead to a weakening of the isolation because the ceramic substrate tends to be robust against partial discharge. First of all organic materials (plastic) e.g. circuit boards and compound of transducers will be damaged.

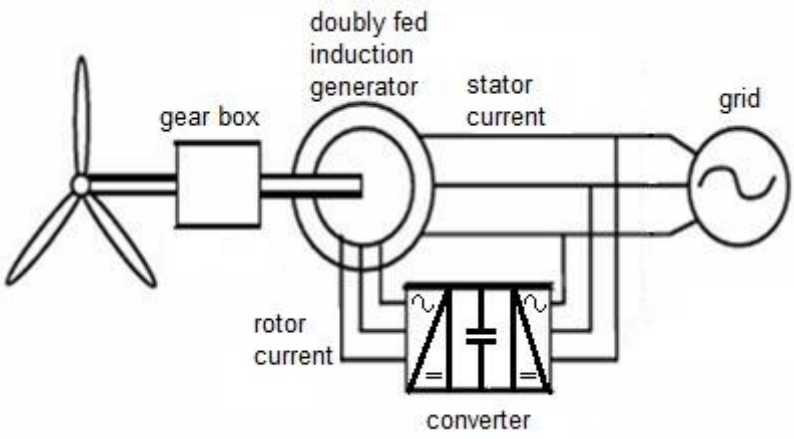
Since every isolation test may cause a premature damage to the module as a result of partial discharge, the number of tests should be kept low. If they cannot be avoided, however, a regeneration time of at least 10 minutes must be kept between 2 subsequent tests and the repeated isolation voltage tests should be performed with reduced voltage. The test voltage must be reduced by 20% for each repeated test.

Please note: The F-option must be removed during the IVT (mounting instruction on request). Then the normal test procedure as above described should be performed.

7.7 FRT (Fault Ride Through) - Function

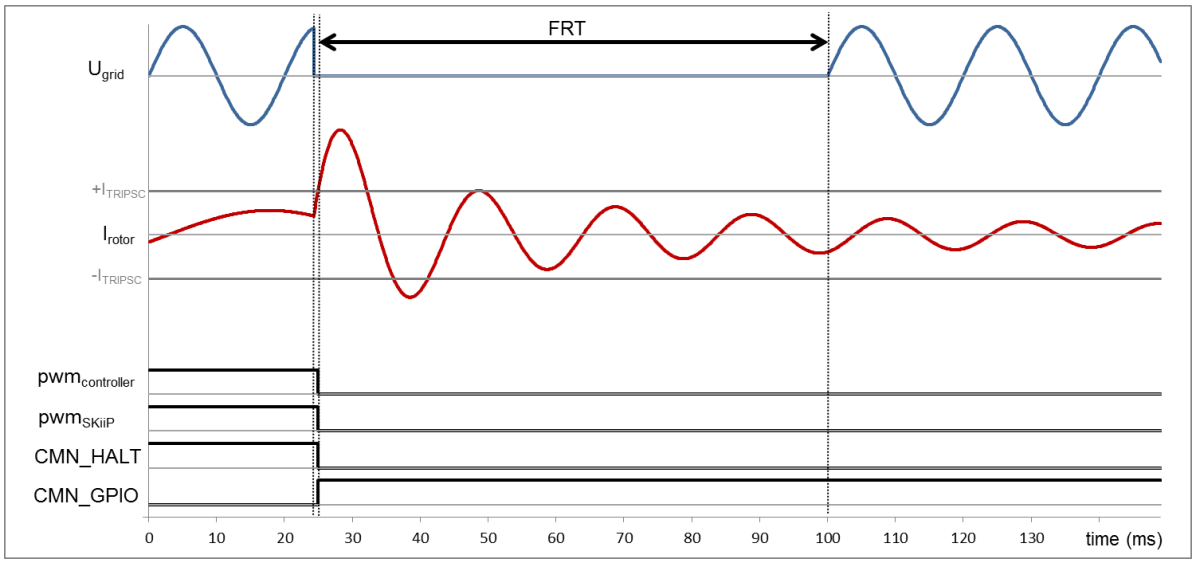
A typical SKiiP 4-application is a converter for wind turbines. It is state of the art that turbines must fulfill grid code requirements for the connection to the electric power system. Parts of this requirements are known as Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT).

Figure 49: Graphic schematic of the wind mill



When doubly fed induction generators are used only the rotor current is controlled by the converter.

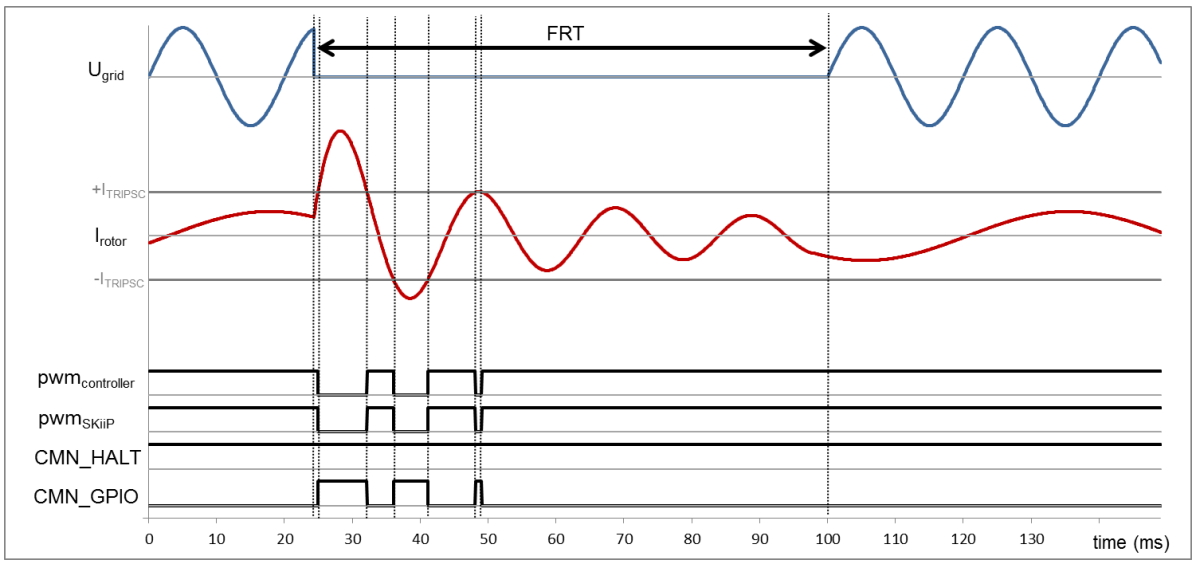
Figure 50: Graphic presentation of SKiiP 4 behavior without FRT-function activated in case of overcurrent



In case of an FRT or LVRT the rotor current can increase to levels higher than the overcurrent trip level of the SKiiP (I_{TRIPSC}) and the SKiiP will trip. Consequentially the PWM of the IGBTs (pwm_{SKiiP}) is interrupted by the SKiiP-driver itself regardless of whether the PWM from the customer controller ($pwm_{controller}$) is running. The SKiiP-driver sets the CMN_HALT-signal to LOW and the CMN_GPIO1-signal to HIGH. The interrupt of the pwm_{SKiiP} is released after the error memory reset time t_{pRESET} has elapsed and if the switching input signals HB_TOP and HB_BOT are set to LOW. In most cases t_{pRESET} is too high to fulfill the grid code requirements.

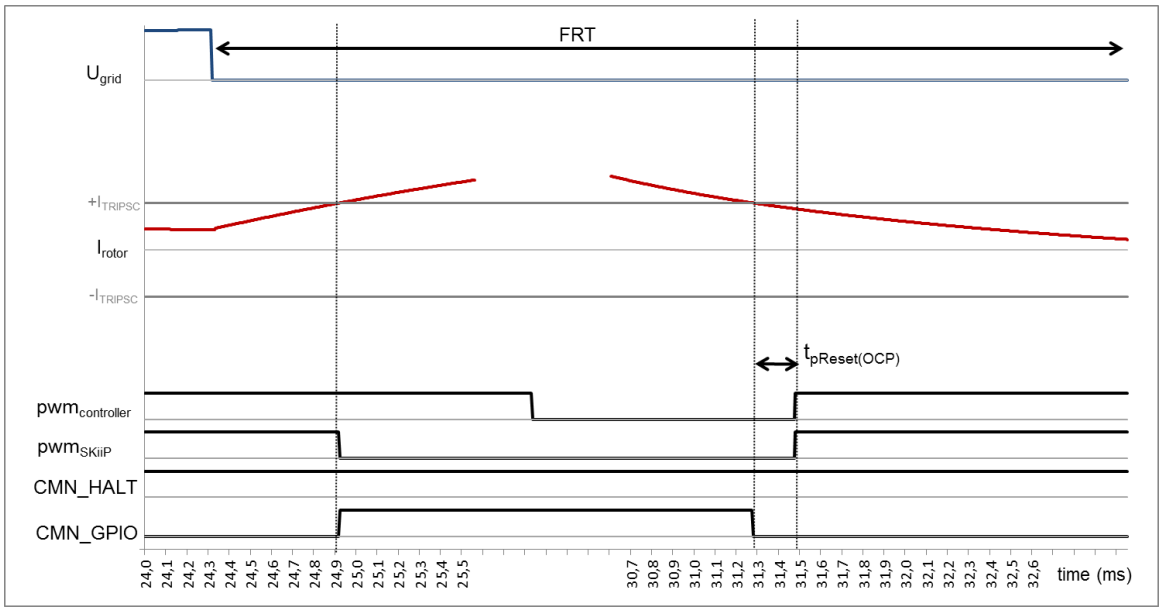
If the FRT-function is activated the error-handling of the SKiiP will be changed and the grid code requirements can be fulfilled. In this case CMN_GPIO1 will not be the inverted CMN_HALT signal anymore. An overcurrent trip will never set CMN_HALT to LOW and it is never stored in the SKiiP error memory.

Figure 51: Graphic presentation of SKiiP 4 behavior with FRT-function activated in case of overcurrent



If the rotor current I_{rotor} exceeds the level I_{TRIPSC} the SKiiP-driver will interrupt the pwm_{SKiiP} and will set the signal CMN_GPIO1 to HIGH as long as I_{TRIPSC} is exceeded. The $pwm_{controller}$ must be turned off. After a period $t_{pReset(OCP)}$ of 200µs which starts after I_{rotor} is below I_{TRIPSC} and $pwm_{controller}$ is turned off, the SKiiP is enabled to start switching as long as the overcurrent trip level is not exceeded again.

Figure 52: Graphic presentation of the driver processing in FRT-case



The freewheeling diodes conduct the rotor current I_{rotor} during the period of blocked pwm_{SKiiP}. The user must take care that the diodes will not be overloaded thermally, because the SKiiP's overcurrent protection is deactivated and the thermal protection is not able to protect the diodes in this FRT operation. Thermal calculations or simulations are necessary to confirm that the SKiiP diodes will not be overloaded. The FRT-Function can be activated through the CAN-Bus interface. Please refer to the CAN user's manual documentation for further details.

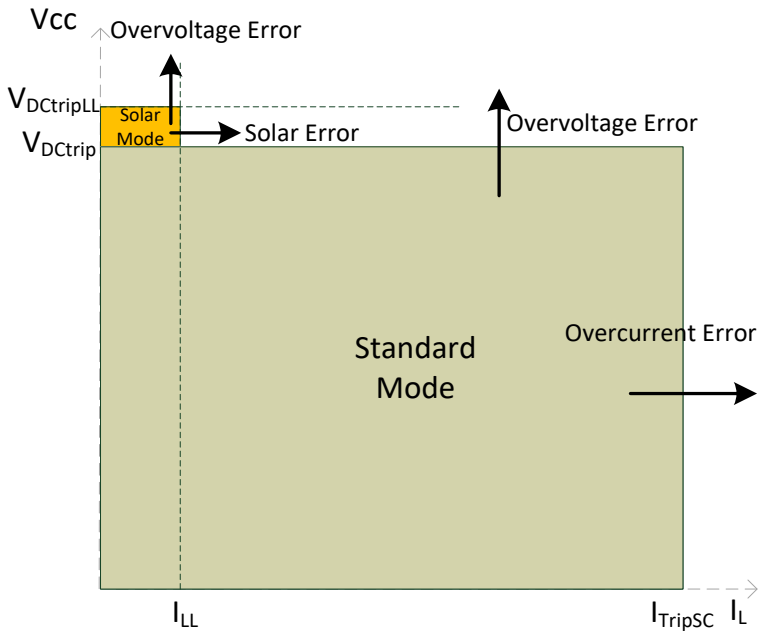
7.8 Solar function

For an operation of the SKiiP 4 during the startup phase typically in PV-solar applications, a higher DC-link voltage trip level must be available for low load currents in contrast to standard applications. A special modification of the current SKiiP 4 1700V type has been carried out to fulfill this specific requirement of the PV-solar market.

Please note: The solar function cannot be activated through CAN and, hence, a dedicated SKiiP®4 for such PV-solar specific operation must be ordered.

The Safe Operating Area (SOA) diagram of the PV SKiiP 4 is indicated in the Figure 53. While the SOA for the standard SKiiP 4 (shown in the Figure 42) is limited by the over voltage trip level V_{DCtrip} and over current trip level I_{TRIPSC} , the modified SOA of the PV SKiiP 4 employs an extended area above V_{DCtrip} and limited by the low load current I_{LL} and a higher over voltage trip level $V_{DCtripLL}$. This operation mode is called "solar mode" and is marked orange in the right diagram of Figure 53. Parameters I_{LL} and $V_{DCtripLL}$ are given in the data sheets SKiiP 4 Solar. The operation at DC-link voltages higher than the recommended voltage levels and especially in this "solar mode" extended SOA is very time limited since the probability of a cosmic ray induced fault increases exponentially under such conditions.

Figure 53: SOA for SKiiP 4 Solar



The operation modes for SKiiP 4 solar are listed in the Table 19.

Table 19: Operation modes SKiiP 4 solar			
Operation mode	**DC-voltage**	**Load current**	**Processing**
Standard mode	$V_{DC} < V_{DCtrip}$	$I_{Load} < I_{trip}$	Hard Switch-off
Solar mode	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} < I_{LL}$	Switch off with IntelliOff
Error mode		$I_{Load} > I_{trip}$	Switch off with IntelliOff, over current error indicated
	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} > I_{LL}$	Switch off with IntelliOff, solar mode error indicated if previous mode was solar mode
	$V_{DCtrip} < V_{DC} < V_{DCtripLL}$	$I_{Load} > I_{LL}$	Switch off with IntelliOff, over voltage error indicated if previous mode was standard mode.
	$V_{DC} > V_{DCtripLL}$		Switch off with IntelliOff, over voltage error indicated

In case the SKiiP 4 is in solar mode (see Table 19) and at DC-Link voltage $V_{DC} > V_{DCtrip}$ the load current I_{Load} exceeds I_{LL}, the solar mode error will be indicated. In this case SKiiP®4 comes into error mode: the SKiiP-driver sets the CMN_HALT-signal to LOW and the CMN_GPIO1-signal to HIGH. The interrupt of the operation mode is released after the error memory reset time t_{pRESET} has elapsed and the switching input signals HB_TOP and HB_BOT are set to LOW.

The solar mode error can be read out by the available CANopen diagnostic software (GUI). In the case of this error, both error bits 13 (over current) and 14 (DC-Link error) will be set. Please refer to the Technical Explanation CANopen SKiiP4, "Error recording", for more details.

Suitable snubber capacitors must be used in case the maximum blocking voltage V_{CES}/V_{RRM} is exceeded. Please refer to chapter 7.6 for further information.

For safe operation the interlock time t_{TD} is increased to a value 4.5 µs in solar mode (Ref. diagram of Figure 53).

Please note: The load must be connected symmetrically, and the load inductivity must be not less than 6µH.

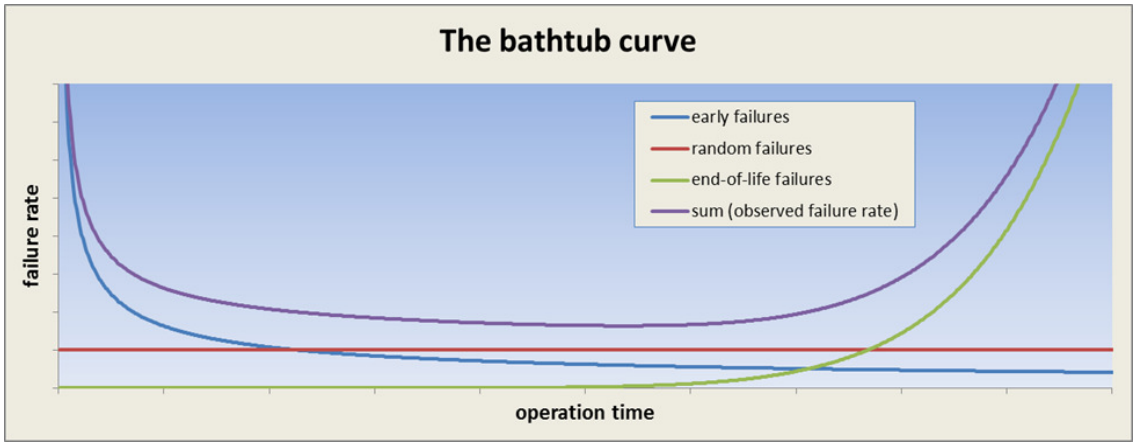
The deactivation or change of the DC-Link trip level via CAN bus is not possible for the Solar SKiiP 4. The activation of the FRT-Function via CAN bus is possible (Please see Technical Explanation CANopen SKiiP4).

7.9 Recommended temperature rating

Please note: The compliance to the temperature characteristics recommended in this chapter are extremely important for the SKiiP 4 reliability and therefore for the long lifetime of the product.

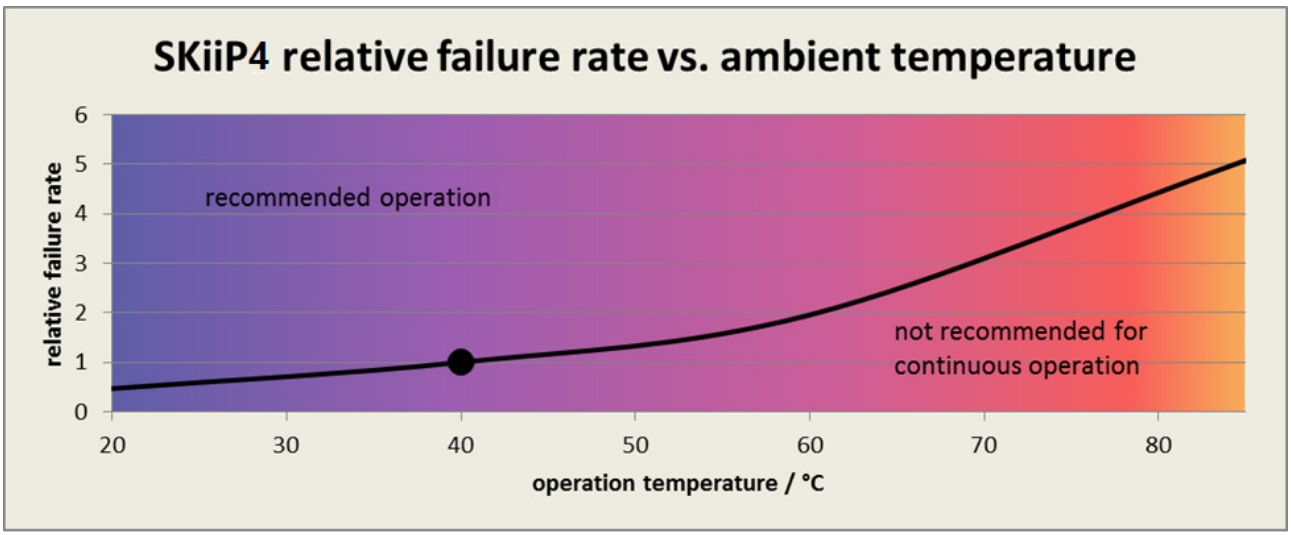
The indicated failure rate describes the probability of the occurrence of a failure within a certain time span. Usually, the failure rate follows a so-called bathtub curve, shown in Figure 54: High in the beginning (failures known as early failures), then dropping to a low and more or less constant value (the random failures) before it rises again as wear-out begins to set in and end-of-life failures set a limit to the useful life of a component.

Figure 54: Probability of a failure during operation time



The evaluation of the failure rate for different temperatures shows that its expected failure rate roughly doubles for a 20 C increase in operating temperature (see Figure 55).

Figure 55: SKiiP driver failure rate temperature dependence calculated according to SN29500



The less stress a device is subjected to, the less likely it is to fail. Low operation time, low current, low temperature, and low dc-link voltage prolong the component's life and, hence, reduce the failure rate. Therefore, the design objective for the individual equipment represents a suitable compromise between exploiting the electrical and thermal capability of a device and obtaining an acceptable failure rate and lifetime expectation.

The following temperature rating is recommended for the SKiiP 4 systems:

- Power section: It is necessary to ensure by calculations and measurements that the recommended IGBT and diode junction temperatures are not exceeded at maximum overload conditions stipulated by the application. The recommended maximum junction temperature under worst case conditions is 150°C being 25°C lower than the maximum permitted chip temperature of 175°C. That margin provides a certain minimum to ensure a reliable operation. Dedicated calculations shall be carried out by the Semikron Danfoss simulation tool SEMISEL which is available on the Semikron Danfoss homepage www.semikron-danfoss.com. Load cycles and cooling conditions can be adapted to meet the application conditions. The measurement of the DCB-sensor temperature (available at the driver connector as analogue voltage signal) can provide a first indication that the system operates as simulated.
- Gate driver: Although the gate drive circuit can operate at ambient temperatures of up to Ta = 85°C, it is recommended that the average ambient temperature of the driver board usually does not exceed 40°C. Lowering the gate driver temperature can be achieved by an additional air forced cooling of the SKiiP's

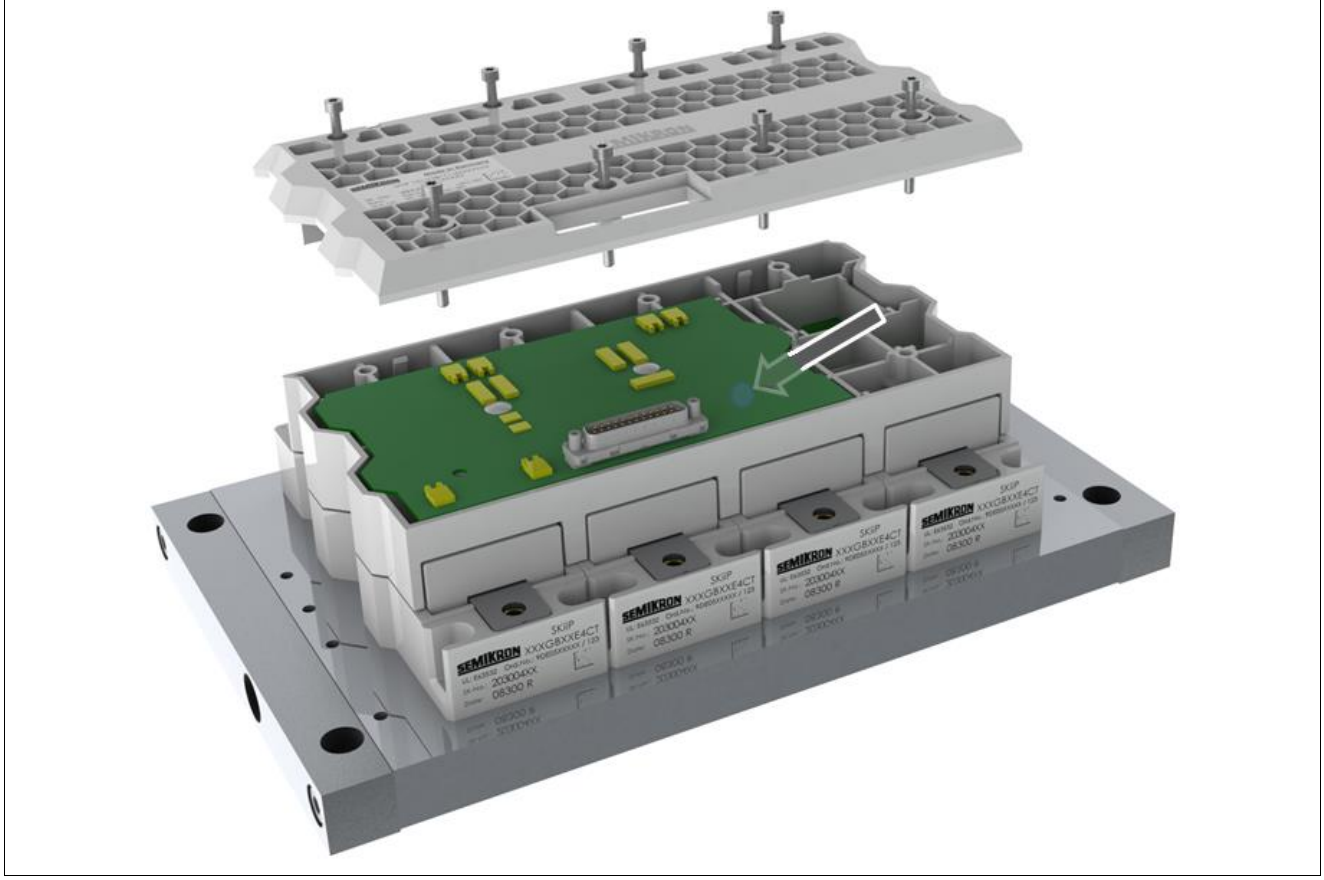
housing. The actual temperature of the gate driver Tdriver in situ could be measured by means of a temperature sensor located at the bottom side of the driver PCB (see Figure 56). The value of the sensor could be read out via CAN-bus interface (please refer to the CANopen documentation for further information). If the temperature exceeds the TDriver Trip given in the SKiiP 4's data sheet the switching operation will be blocked and an error signal will be issued correspondingly. The default values for the TDriver Trip are provided in Table 20.

Table 20: Default values for the $T_{Driver\ Trip}$

	Min. Value	Typ. Value	Max. Value
$T_{Driver\ Trip}$	113	115	124

If necessary the trip level of the temperature sensor can be adjusted to a lower level by the CAN-bus interface.

Figure 56: Position of the driver temperature sensor SKiiP 4



7.10 Switching operation and current sharing between paralleled half bridge modules

The SKiiP 4 is made for switching application. However, since dynamic processes are occurring in the utilized semiconductors, e.g. IGBT and diodes a certain minimum time shall be considered before a next switching operation can be started. Hence this minimum conduction time or pulse width for the IGBT and the Diode shall be kept by the application software to ensure that all transient processes in the semiconductors have been finished and no undesired tripping or oscillation might happen. For further details please refer to application handbook section 2.3.3.2. For the SKiiP 4 the following minimum conduction times shall be kept:

- For 1200V SKiiP4
  - t_{min} (IGBT) > 2µs
  - t_{min} (Diode) > 3µs

- For 1700V SKiiP4
  - t_{min} (IGBT) > 2µs
  - t_{min} (Diode) > 5µs

The busbar has to be designed symmetrically to make sure that the current sharing is equal. Unequal current sharing can overload single half bridge modules and leads to imbalance during switching operation as well as in steady state conduction which can finally destroy the power section.

Symmetrical AC and DC-link design leads to equal stray inductances between the half bridge modules which ensures balanced commutation and current sharing. Each half bridge module has to have the same stray inductance to the DC-link capacitors.

The recommended AC connection is shown in Figure 57. The current sharing should be measured in the design phase by "double pulse testing" (see AN-7006) and in the final design under real operation conditions. This can be done e.g. by Rogowski current sensors which are located around the DC+ and DC-terminals.

7.11 Paralleling of SKiiP®4

The parallel operation of SKiiP 4's requires the following considerations and features:

- Common error management for all paralleled SKiiP 4 can be realized using the HALT signal
- Monitoring of analogue signals, e.g. temperature or current
- one power supply should be used for all subsystems

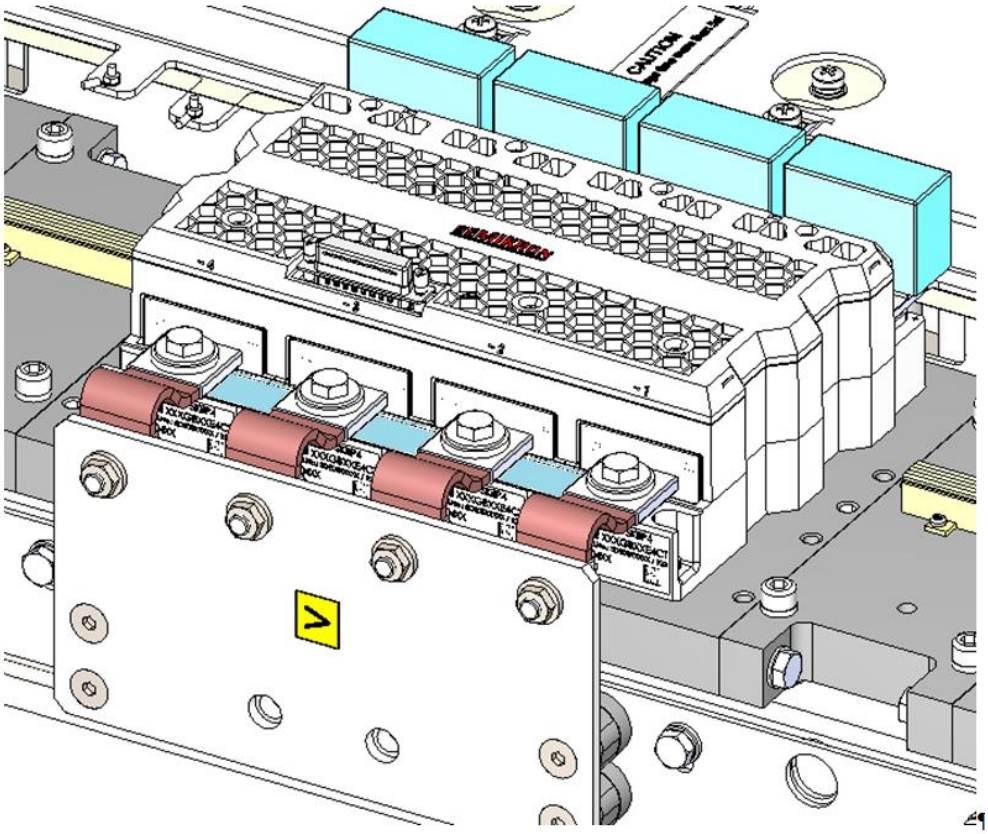
By using paralleled SKiiPs it has to be made sure that no SKiiP will be overloaded, e.g. by current imbalance. Such an inhomogeneous current can be caused by different output voltages of the paralleled inverters which could be a consequence of:

- different propagation time of driver board signals
- different switching times of power semiconductors
- tolerance of forward voltage drop of IGBT or diodes
- different DC link voltage levels
- different cooling conditions of paralleled half bridges (e.g. in air cooled applications with thermal stacking)
- different external impedance

A suitable parallel connection of all AC-terminals can be achieved by an additional flexible **cross connector** directly mounted on the SKiiP AC terminals (marked with an arrow in Figure 57).

Please note that the current rating of this bar must not be very high, because there is no load current flowing in this bar. There are only high frequency currents flowing. Thus the flexibility can be achieved by using a comparatively thin material.

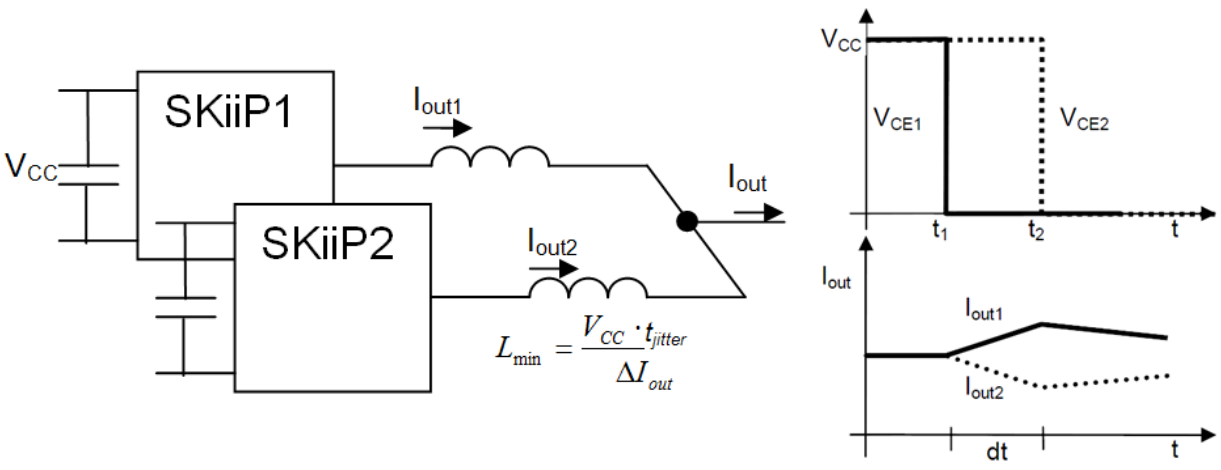
Figure 57: An example of SKiiP 4 AC terminal parallel connection



To minimize the above mentioned effects the system designer has to make sure, that there is sufficient inductance between the AC output terminals of the paralleled SKiiP subsystems. The impedance has two tasks:

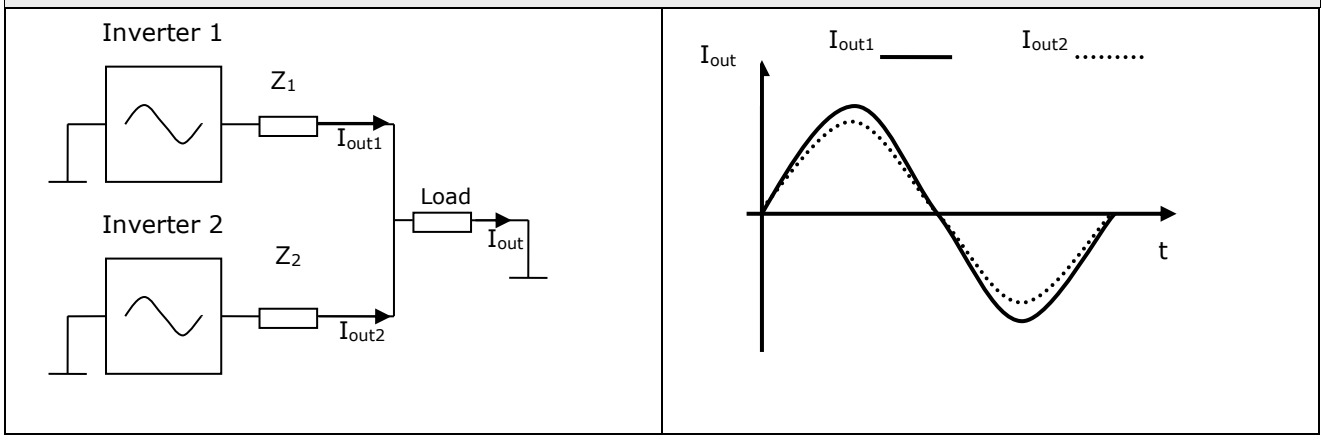
- On one hand it should prevent from the generation of an imbalance current during the switching moment. That could lead to different switching loss and in severe cases to undesired oscillations. This is shown in Figure 58. The value t_{jitter} is given in the SKiiP 4 data sheet on page 2.

Figure 58: Effects of paralleling SKiiP 4



- On the other hand a different root mean square value of the output current should be avoided. Symmetric effects come from the inductivities (AC choke) and the Ohmic resistors (choke resistor, wiring resistor and path resistance) as shown in Figure 59.

Figure 59: Schematic circuit diagram



Tolerances of forward voltage drop of IGBT or diodes

The IGBTs used in the SKiiPs have a positive temperature coefficient. The freewheeling diodes are produced with a small forward voltage tolerance range. Both features limit an inhomogeneous current distribution. No further selection of forward voltage selection is necessary.

Different DC link voltage levels

To avoid different output voltages caused by different DC link voltages levels, the DC link should be connected in parallel. Furthermore oscillations between such interconnected capacitor banks must not occur. For large systems fuses between the capacitor banks are recommended. The paralleled systems should have the same DC link with the same capacitor type and capacitor values.

Different cooling conditions of paralleled half bridges

The cooling system of the paralleled SKiiP units should be designed in way to avoid thermal stacking.
In spite of all the mentioned actions it has to be taken into account that for remaining imbalanced current sharing a derating of the nominal current of the power stage has to be considered.

Different production lot

In general, besides all the before mentioned constraints it is not recommendable although not impossible to parallel SKiiP4 of different production lots. Typically, the relevant parameter for an advantageous paralleling differs less when SKiiPs of one production lot are utilized in parallel.

Provisions for minimum switching pulse and conduction time

In a parallel connection of SKiiP4 it is essential to follow the specified minimum durations for on and off time to ensure error free operation. For further details please refer to chapter 7.10.

7.12 Prevention of condensation

A condensation of humidity in the environment where the SKiiP is located must be avoided. This can be ensured by control of air or water flow so that the heat sink temperature is always higher than ambient temperature. Hence, the utilization of a chilled coolant is therefore not recommended. Condensation may also occur because of a day/night temperature change. If the power electronic equipment was exposed to humidity or moisture during transport and storage, it should be sufficiently dried before commissioning. This can be done by air heater in air cooled systems or by pre-heated water in water cooled systems before connecting the operation voltage to the SKiiP.

8. Logistics

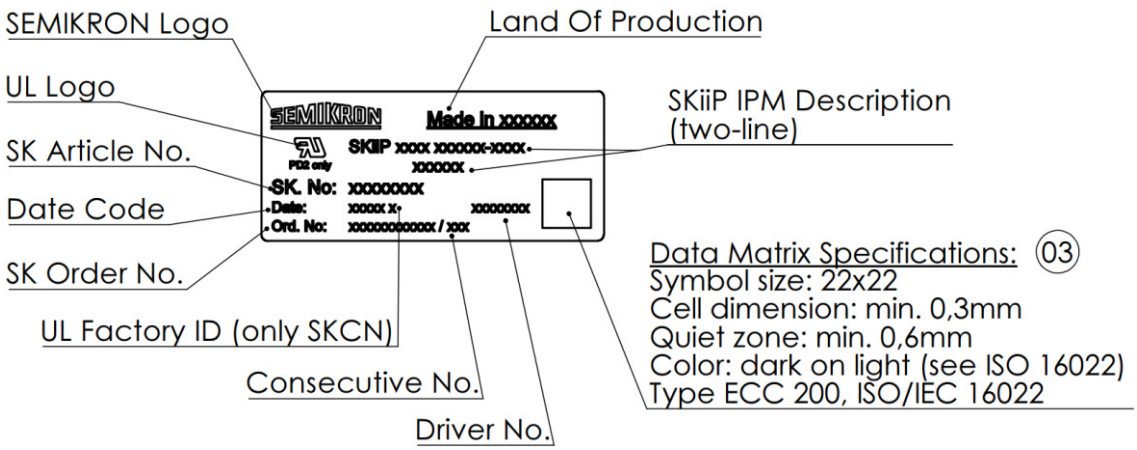
8.1 Label

For reasons of traceability all SKiiP 4 modules are marked with a system, half bridge, driver shuttle and a warranty label.

8.1.1 System Label

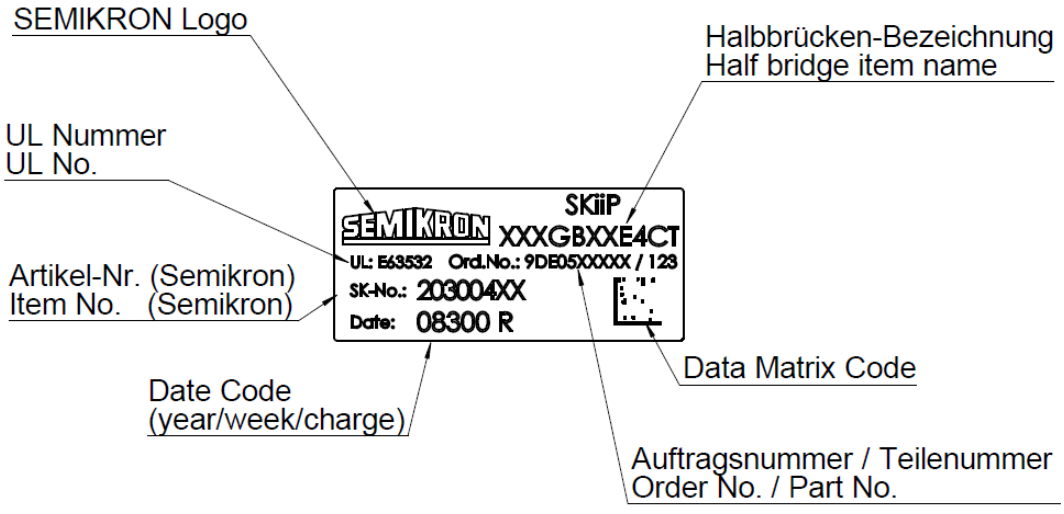
The system label of the SKiiP (Figure 60) contains all information necessary for customers to clearly identify the product. In case of technical inquiries please always refer to the SKiiP Item number written on this label.

Figure 60: System Label of SKiiP 4



8.1.2 Half-Bridge Laser Label

Figure 61: Half bridge label of SKiiP 4



8.1.3 Warranty Label

The warranty label is shown in Figure 62. The position of the warranty label can be found in the corresponding data sheet.

Figure 62: Warranty Label of SKiiP 4

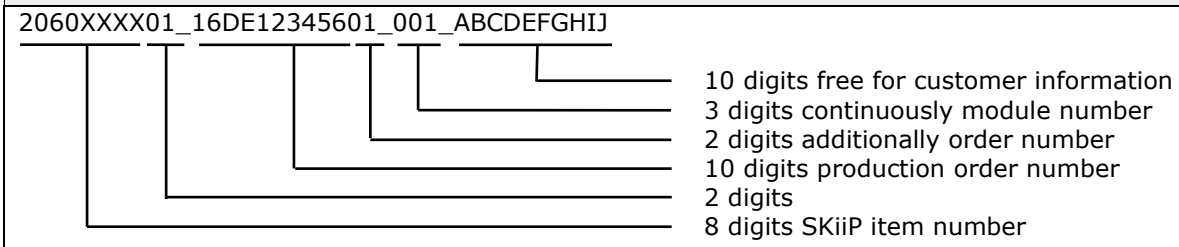
Please note: Removing the warranty label will result in loss of warranty in case of product reclamation.

8.1.4 Matrix Code

The Data Matrix Code is described as follows:

- Cell size: 0.3mm
- Read distance: 60 – 100 mm
- Max. angle of 30° (vertical reference line) for reading

Figure 63: Data Matrix Code of SKiiP 4 (example)



8.1.5 Provisions and handling after use

Components which are obsolete or defective must be disposed according to local regulations.

Figure 1: SKiiP 4 – 4 fold 3
Figure 2: Half bridge definition 4
Figure 3: Half bridge "exploded assembly view" 4
Figure 4: Main terminals construction principle 5
Figure 5: Type Designation Code 6
Figure 6: Schematics of Grounded Delta Grid and Star Grounded Circuit Network 9
Figure 7: Implementation of additional basic isolation between SKiiP 4 driver interface and controller board 11
Figure 8: Gate Driver Board block diagram 13
Figure 9: Gate Driver Interface 14
Figure 10: SKiiP 4 - connector D-Sub 25 pin, male plug, vertical, top view 14
Figure 11: Overview schematics SKiFace interface (CMN_GPIO1/2 and CMN_HALT are not shown 17
Figure 12: TOP/BOT PWM Signal Input 19
Figure 13: Threshold level for HB_TOP and HB_BOT 19
Figure 14: Schematic view of the analogue output signals 20
Figure 15: Application example – symmetric wired differential amplifier. Terminal description HB_I and HB_I_GND for current measurement 21
Figure 16: Application example of the HALT signal processing for separated SKiiP 4 systems 23
Figure 17: Application example of the CMN_GPIO1 (inverted HALT signal) as error output signal 24
Figure 18: CAN-Interface 25
Figure 19: CAN – application example for several SKiiP 25
Figure 20: Prevention of ground loops by differential amplifier circuitry 26
Figure 21: Ground and shield connection. Principle schematics for Ground and shield connection. Principle equivalent circuit of switching signal inputs 27
Figure 22: Ground and shield connection. Principle equivalent circuit for analogue output signals (Example: Temperature output) 27
Figure 23: Connection of reserved and not used signals at the user controller board 28
Figure 24: Power-On-Reset timing diagram 29
Figure 25: Short pulse suppression 31
Figure 26: Turn-off speed scenarios 31
Figure 27: Switching frequency range 34
Figure 28: Timing diagram for the TOP/BOT overlapping error processing (t<3µs) 34
Figure 29: Timing diagram for the HB_TOP/HB_BOT overlapping error processing (t>3µs) 35
Figure 30: Short circuit cases 36
Figure 31: Characteristics between current and the voltage at HB_I, SKiiP 4 3-fold) 37
Figure 32: Characteristic between current and the voltage at HB_I, SKiiP 4 4-fold 37
Figure 33: Characteristic between current and the voltage at HB_I, SKiiP 4 6-fold 38
Figure 34: Bode diagram of the AC-current measurement at the SKiiP 4 interface 39
Figure 35: Compensation principle of SKiiP 4 current sensor 39
Figure 36: Characteristic between DCB-sensor temperature and the voltage at CMN_TEMP 40
Figure 37: DC link voltage sensor output 1200V system 41
Figure 38: DC-link voltage sensor output 1700V system 42
Figure 39: Bode diagram of the DC-link voltage measurement at the SKiiP 4 interface 43
Figure 40: Maximum forces at the main terminals 44
Figure 41: AC connection 45
Figure 42: Safe Operating Area for standard SKiiP 4 46
Figure 43: Definition of thermal resistances 47
Figure 44: Sensor position in SKiiP 4 GB (6fold, 4fold, 3fold) with proposed cooling (water inlet) direction 48
Figure 45: SKiiP 4 side cap mechanical drawing 49
Figure 46: Description of fitting ISO 1179-2 — G 1/2 A — L 50
Figure 47: Description of fitting ISO 1179-3 — G 1/2 A — G 50
Figure 48: Graphic presentation of the electrical connections by the IVT procedure 51
Figure 49: Graphic schematic of the wind mill 52
Figure 50: Graphic presentation of SKiiP 4 behavior without FRT-function activated in case of overcurrent 53
Figure 51: Graphic presentation of SKiiP 4 behavior with FRT-function activated in case of overcurrent 53
Figure 52: Graphic presentation of the driver processing in FRT-case 54
Figure 53: SOA for SKiiP 4 Solar 55
Figure 54: Probability of a failure during operation time 57
Figure 55: SKiiP driver failure rate temperature dependence calculated according to SN29500 57

Figure 56: Position of the driver temperature sensor SKiiP 4 58
Figure 57: An example of SKiiP 4 AC terminal parallel connection 60
Figure 58: Effects of paralleling SKiiP 4 60
Figure 59: Schematic circuit diagram 61
Figure 60: System Label of SKiiP 4 62
Figure 61: Half bridge label of SKiiP 4 62
Figure 62: Warranty Label of SKiiP 4 63
Figure 63: Data Matrix Code of SKiiP 4 (example) 63

Table 1: SKiiP 4 standard product range 7
Table 2: SKiiP 4 Tests for qualification and re-qualification 8
Table 3: SKiiP 4 Electromagnetic compatibility 8
Table 4: : SKiiP 4 Isolation limits 9
Table 5: Altitude Correction Factors (IEC 60664-1) 10
Table 6: Installation altitudes for SKiiP 4 as function of the grid configuration, overvoltage category and required isolation degree 12
Table 7: Pin configuration SKiiP 4 15
Table 8: Requirements to the auxiliary power supply 18
Table 9: Ground connections of SKiiP 4 26
Table 10: IntelliOff functionality 32
Table 11: Power loss impact of IntelliOff operation 32
Table 12: Error delay time 33
Table 13: Signal characteristics of Under Voltage protection of the primary side 33
Table 14: Signal characteristic of current measurement 36
Table 15: Characteristics of the DCB-temperature sensor circuit 40
Table 16: V_{DC} characteristics 41
Table 17: Maximum allowable forces to terminals 43
Table 18: Snubber capacitors for SKiiP 4 46
Table 19: Operation modes SKiiP 4 solar 56
Table 20: Default values for the $T_{Driver\ Trip}$ 58

9. Abbreviations

Abbreviation	Meaning
CTE	Coefficient of Thermal Expansion
DBC	Direct bonded copper
D-Sub	D-Subminiature
EMC	Electromagnetic compatibility
FRT	Fault Ride Through
FwDi	Free-wheeling diode
GB	halfbridge configuration
GND	Ground
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
IVT	Isolation Voltage Test
PCB	Printed Circuit Board
PTC	Positive Temperature Coefficent
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
SCP	Short Circuit Protection
SKiiP	Semikron intelligent integrated Power
SPS	Short Pulse Suppression
UVP	Under Voltage Protection
SOA	Safe Operating Area

10. Symbols

Symbol	Meaning
I_{Cnom}	Nominal collector current of IGBT
I_{Fnom}	Nominal forward current of diode
$I_{digiout}$	Digital output sink current (HALT-signal)
Q_{PD}	Charge of the Partial Discharge event
$R_{CC'+EE'}$	Resistance of the interconnections between terminals and die
R_{th}	Thermal resistance
$t_{pReset(OCP)}$	Overcurrent reset time
t_{jitter}	Jitter clock time
t_{SIS}	Short pulse suppression time
t_{bl}	Blanking time
t_{POR}	Power-On Reset time
T_a	Ambient temperature
T_j	Junction temperature
T_r	Temperature at reference position
U_{LE}	Line to earth voltage
U_{LL}	Line to line voltage
V_{CEstat}	Collector-Emitter Threshold Static Monitoring Voltage
$V_{it+\ HALT}$	Input threshold voltage HALT-signal (HIGH)
$V_{it-\ HALT}$	Input threshold voltage HALT-signal (LOW)
$T_{DriverTrip}$	Over temperature trip level
$f0_{Uana}$	Bandwidth of DC-voltage measurement @ VDctrip
$f0_{Iana}$	Bandwidth of current measurement @ ITRIPSC
$f0_{Tana}$	Bandwidth of temperature measurement @ Ttrip

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors"

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[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3

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Semikron Danfoss International GmbH

Sigmundstrasse 200, 90431 Nuremberg, Germany

Tel: +49 911 65596663

sales@semikron-danfoss.com, www.semikron-danfoss.com