

Revision:	01
Issue date:	2026-09-15
Prepared by:	Claire Garnier
Approved by:	Andreas Giessmann

Keyword: SKiiP, Parallel Board

SKiiP4 Paralleling

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1. Introduction

The increasing power demands of modern applications, such as high-performance motor drives, renewable energy inverters, and industrial power supplies, often exceed the capacity of a single power module. Paralleling multiple SKiiP4 Intelligent Power Modules (IPMs) is an effective and scalable strategy to meet these high-current requirements. However, achieving a robust and reliable parallel operation requires careful attention to electrical and thermal design to ensure proper current sharing and system stability.

By using SKiiPs in parallel it has to be made sure that no SKiiP will be overloaded due to current imbalance. Inhomogeneous current can be caused by different output voltages of the paralleled inverters which could be a consequence of:

1. Tolerance of forward voltage drop of IGBT or diodes
2. Different DC link voltage levels
3. Different cooling conditions of paralleled half-bridges
4. Different external AC impedance
5. Different propagation time of driver board signals
6. Different switching times of power semiconductors

Points 1 to 4 are described in chapter 2 of this document. Parallel Boards from Semikron-Danfoss have been designed and qualified to address the points 5 and 6 and are described in chapter 3.

2. Key Considerations for Paralleling

Only SKiiPs with the same heatsink type and the same number of folds may be operated in parallel. If SKiiPs with different part numbers (P/Ns) must be connected in parallel, please contact a Semikron Danfoss application engineer to verify the feasibility of the proposed configuration.

2.1 Forward voltage drop tolerances of IGBTs and diodes

The SKiiPs are designed to promote balanced current sharing. This is achieved because the IGBTs have a positive temperature coefficient, which naturally counteracts thermal runaway, and the freewheeling diodes are produced with a tight forward voltage tolerance. Together, these characteristics limit uneven current distribution between parallel modules.

2.2 Symmetrical DC-link connection

To ensure a common voltage level and prevent output discrepancies, the DC links of the parallel units must be interconnected. This design must also prevent oscillations from occurring between the capacitor banks. For large systems, installing fuses between the capacitor banks is recommended for protection.

For balanced performance, the entire parallel system must be symmetrical. This requires using identical capacitor types and values, as well as identical high-current connections (busbars) for both the DC+ and DC- paths.

2.3 Thermal management

Since IGBTs and diodes parameters are temperature-dependent, cooling has an influence on the static and dynamic current symmetry.

For this reason, the cooling system must be designed to prevent thermal stacking, ensuring that the heat dissipated by one SKiiP does not raise the temperature of adjacent units. With Si diodes, a temperature difference of 10K means around 20mV difference in the forward voltage of the same diodes. The diode's negative temperature coefficient then causes the hotter diode to draw even more current, further widening the temperature gap.

In conclusion, SKiiPs that are electrically connected in parallel must not be thermally connected in series.

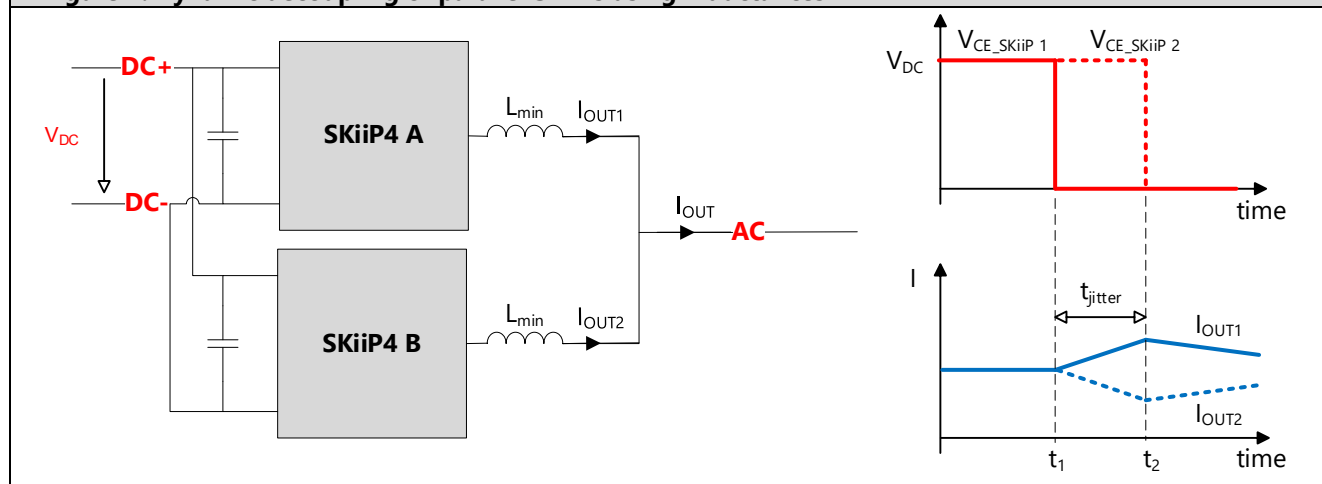
2.4 AC output connection

The system designer has to make sure that there is sufficient inductance between the AC output terminals of the paralleled SKiiPs. The minimum inductance value is defined as follows:

$$2 \cdot L_{min} = \frac{V_{DC} \cdot t_{jitter}}{\Delta I_{out}}$$

The value t_{jitter} is given in the SKiiPs datasheets. It is the same value for all SKiiP4 variants.

Figure 1: Dynamic decoupling of parallel SKiiPs using inductances



The impedance serves two primary functions:

- Preventing an imbalanced current during switching, which can cause differential switching losses and, in severe cases, undesired oscillations.
- Correcting differences in the RMS value of the output current. An AC choke and its associated ohmic resistance (from the choke and cables) can reduce existing current asymmetry.

For an application using two SKiiP 2414 GB17E4-4DUHP in parallel, with a worst-case working point of 1100V DC voltage, 350A output current per SKiiP and an acceptable imbalance of 30A between the SKiiPs, the minimum inductance value is calculated as follows, based on datasheet values:

Figure 2: Extract of the datasheet SKiiP 2414 GB17E4-4DUHP

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
t_{jitter}	jitter clock time		50	58	ns

$$2 \cdot L_{min} = \frac{1100V \cdot 58ns}{30A} = 2.13\mu H$$

$$L_{min} = \frac{1100V \cdot 58ns}{30A} = 1.07\mu H$$

Minimum required inductance value in output for each SKiiP is then 1.07μH.

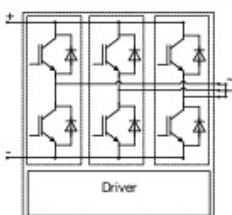
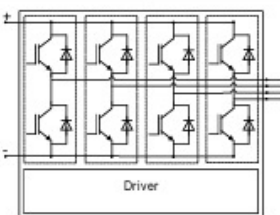
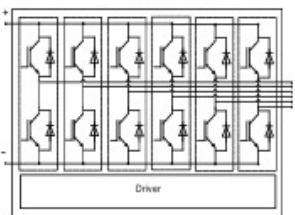
Hard paralleling of SKiiPs (i.e. without output inductor) is possible if the inductance value of the output busbar or cables is higher than the minimum required inductance. This requires symmetrical busbar arrangement on each output. In case output inductors are used, inductance of the busbar/cables can be neglected.

Important note: for low-frequency applications (<5Hz), the inductive share is ineffective in practice. This is because the inductor's impedance, which is proportional to the frequency, becomes negligible and loses its ability to ensure dynamic current balancing during switching events.

3.1 Parallel Board selection guide

Each Parallel Board is compatible with all SKiiP4 GB 1200V and 1700V from Table 1.

Table 1: SKiiP standard product range

3-fold		4-fold		6-fold	
					
SKiiP 1814GB12E4- 3DUW/HP	SKiiP 1814GB17E4- 3DUW/HP	SKiiP 2414GB12E4- 4DUW/HP	SKiiP 2414GB17E4- 4DUW/HP	SKiiP 3614GB12E4- 6DUW/HP	SKiiP 3614GB17E4- 6DUW/HP
					
SKiiP 1814GB12E4- 3DUL	SKiiP 1814GB17E4- 3DUL	SKiiP 2414GB12E4- 4DUL	SKiiP 2414GB17E4- 4DUL	SKiiP 3614GB12E4- 6DUL	SKiiP 3614GB17E4- 6DUL
					
$I_{Cnom} = 1800A$		$I_{Cnom} = 2400A$		$I_{Cnom} = 3600A$	

The SKiiP4 Parallel Board controls up to four SKiiP4 through a single connector. For enhanced EMI protection during the transmission of switching and error signals, an optional fiber-optic adapter (F-option) can be mounted on the board. When using this adapter, you must select the F-option compatible SKiiP4 Parallel Board variant, as listed in Table 2. A separate mechanical housing is not required, as the Parallel Board is designed to be mounted directly onto a metal frame within the cabinet.

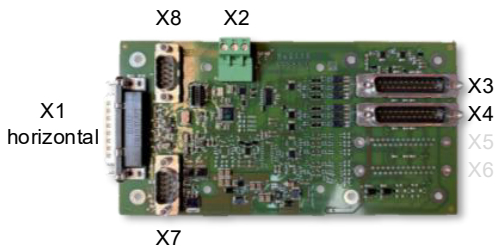
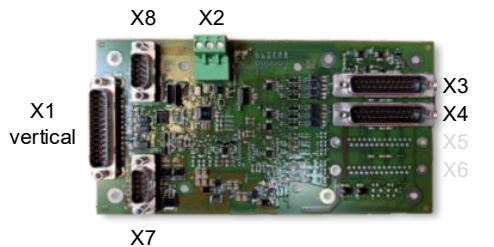
Table 2: SKiiP4 Parallel Board variants

Part number	F-option compatible	Quantity of SKiiPs in parallel
L5064201	No	4
L5064202	No	3
L5064203	No	2
L5064204	Yes (P/N L5066401)	4
L5064205	Yes (P/N L5066401)	3
L5064206	Yes (P/N L5066401)	2

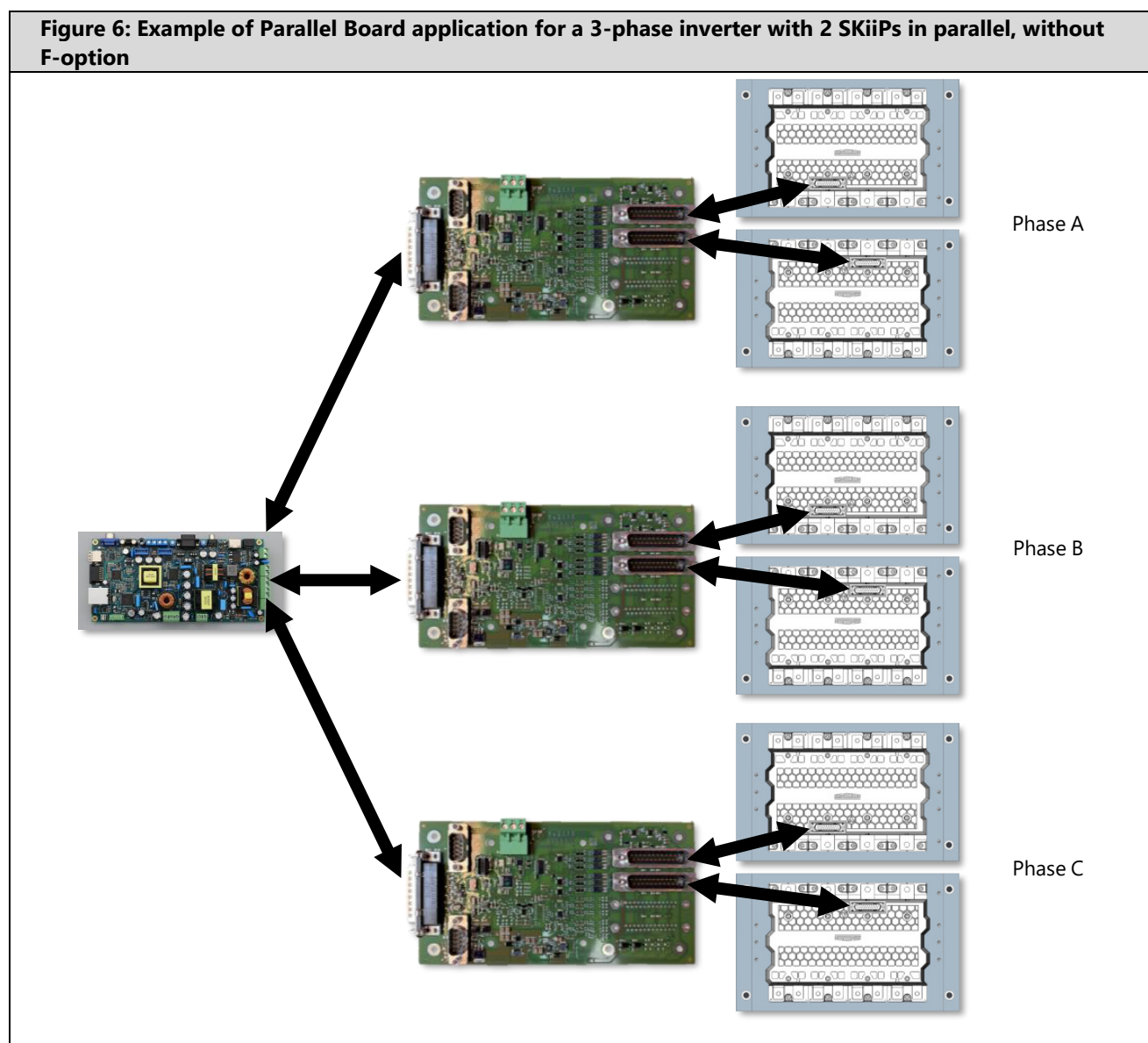
For more information related to fiber optic interface, please refer to "Semikron Danfoss Technical Explanation SKiiP4 F option EN Rev 02".

3.2 Parallel Board overview

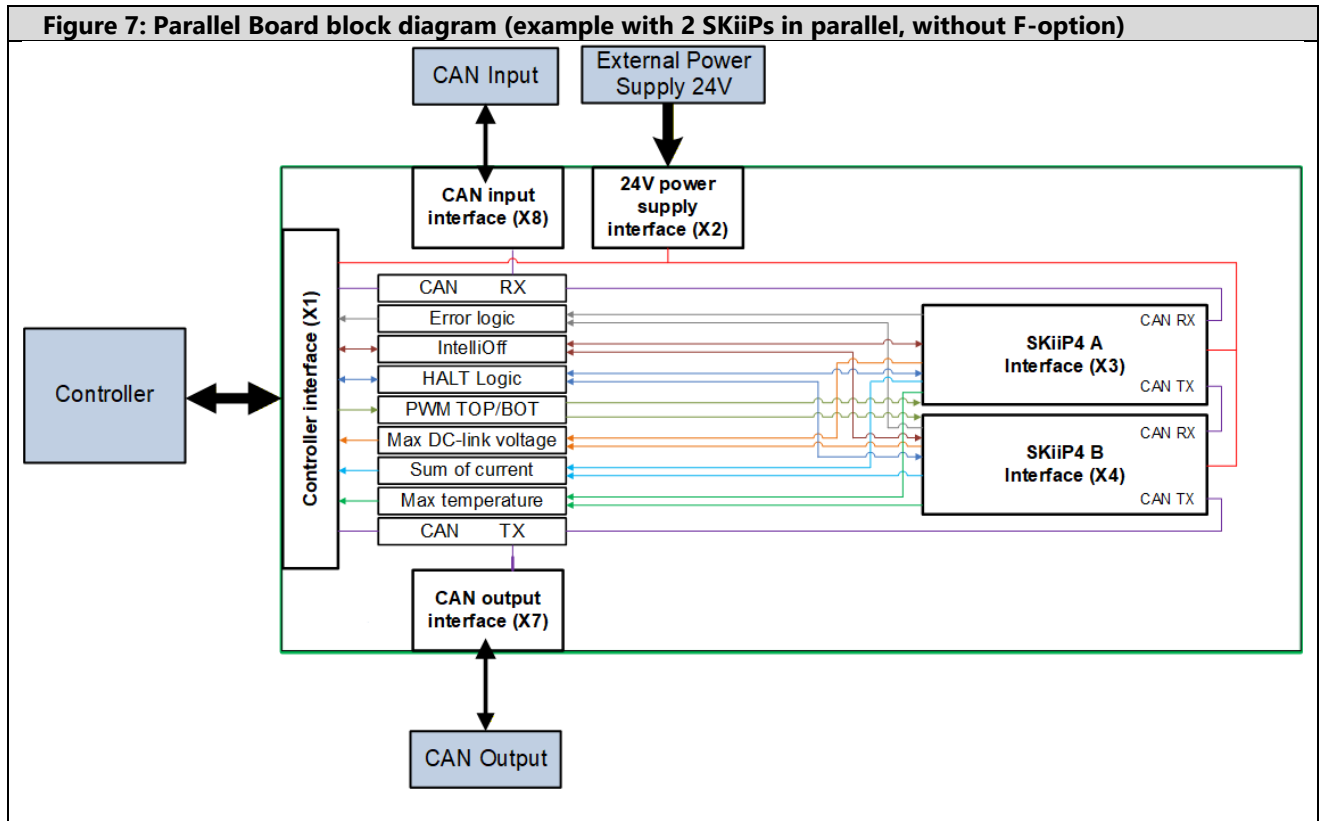
The pictures below show the physical differences between L5064202 (SKiiP4 Parallel Board for 2 SKiiPs in parallel without F-option) and L5064205 (SKiiP4 Parallel Board for 2 SKiiPs in parallel with F-option).

Figure 4: L5064202 SKiiP4 Parallel Board for 2 SKiiPs <i>without</i> F-option	Figure 5: L5064205 SKiiP4 Parallel Board for 2 SKiiPs <i>with</i> F-option
	

Each Parallel Board is driving one electrical phase (I_{out}), e.g., three Parallel Boards are needed for a 3-phase inverter (Figure 6).



The main functions of the Parallel Board are shown in the Figure 7. The details of each interface and function are described in the next paragraphs.



Please refer to "Semikron Danfoss Technical Explanation SKiiP4 EN Rev13" (chapter Gate driver interface SKiiFace) for further information and pin assignment of connections X1, X3, X4, X5, X6.

3.3 External power supply

The supply voltage for SKiiP4 Parallel Board and for all the connected SKiiP4 must be provided exclusively through the power supply connector X2.

Table 3: X2 connector pin assignment			
Pin	Signal name	Function	Specification
1	SHLD_GND	Ground	Internally capacitively coupled to PWR_GND
2	PWR_GND	Ground	
3	+24V	Supply voltage input for Parallel Board and SKiiP4 A to D	See Table 4

Power supply cable should be twisted to enhance the EMI robustness.

3.3.1 Power supply requirements

Table 4: power supply requirements	
Power supply	 24V +/-20% The minimum supply voltage shall be 19,2V measured at SKiiP4 input (considering voltage drop on connection cable between Parallel Board and SKiiP4)
Maximum rise time of 24V	<2s
Rated current	$1.5 \cdot I_S \cdot \text{Number of SKiiPs in parallel}$ For the I_S parameter, please refer to the SKiiP4 datasheet.
Minimum peak current of auxiliary supply	$2 \cdot I_S \cdot \text{Number of SKiiPs in parallel}$ Minimum 6A with 4 SKiiPs in parallel

For an application using three SKiiP 2414 GB17E4-3DUHP in parallel, with a worst-case working point of 200Arms per SKiiP and a 3kHz switching frequency, the rated current for the external power supply for one phase is calculated as follows, based on datasheet values:

Figure 8: Extract of the datasheet SKiiP 2414 GB17E4-4DUHP					
Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
Driver (all values at T=25°C unless otherwise specified)					
V_s	supply voltage non stabilized	19.2	24	28.8	V
I_{S0}	bias current @ $V_s = 24V$, $f_{sw} = 0$, $I_{AC} = 0$		260		mA
I_S	$k_1 = 46 \text{ mA/kHz}$, $k_2 = 0,00015 \text{ mA/A}^2$, $f_{out} = 50\text{Hz}$, sinusoidal current	$= 260$	$+ k_1 \cdot f_{sw}$	$+ k_2 \cdot I_{AC}^2$	mA

$$1.5 \cdot \left(260\text{mA} + 46 \frac{\text{mA}}{\text{kHz}} \cdot 3\text{kHz} + 0.00015 \frac{\text{mA}}{\text{A}^2} \cdot (200\text{A})^2 \right) \cdot 3 = 1.8\text{A}$$

3.3.2 Ground connection

SKiiP4 Parallel Board has the same ground connection as SKiiP4.

3.4 Analog outputs

3.4.1 DBC temperature signal processing

The Parallel Board handles temperature feedback by performing the following function:

- It receives the individual analog temperature signals from each connected SKiiP4.
- It compares all incoming temperature values.
- It outputs the single highest (maximum) DBC temperature value to the controller.

The specifications provided in Table 5 apply only to the SKiiP4 Parallel Board. For details on the SKiiP4's own temperature measurement characteristics, please consult the "Semikron Danfoss Technical Explanation SKiiP4 EN Rev13".

Table 5: signal characteristics of temperature measurement for Parallel Board

Signal characteristics	Value
Output signal	CMN_TEMP/CMN_TEMP_GND at connector X1
Max output current	5mA
Output voltage range	0V to 10V
Analog temperature signal CMN_TEMP @150°C	10V
Analog temperature signal CMN_TEMP @30°C	0V
Signal bandwidth	Max 50Hz
Accuracy of analog signal over full temperature range (ΔI_{OUT} Parallel Board)	+/-3%

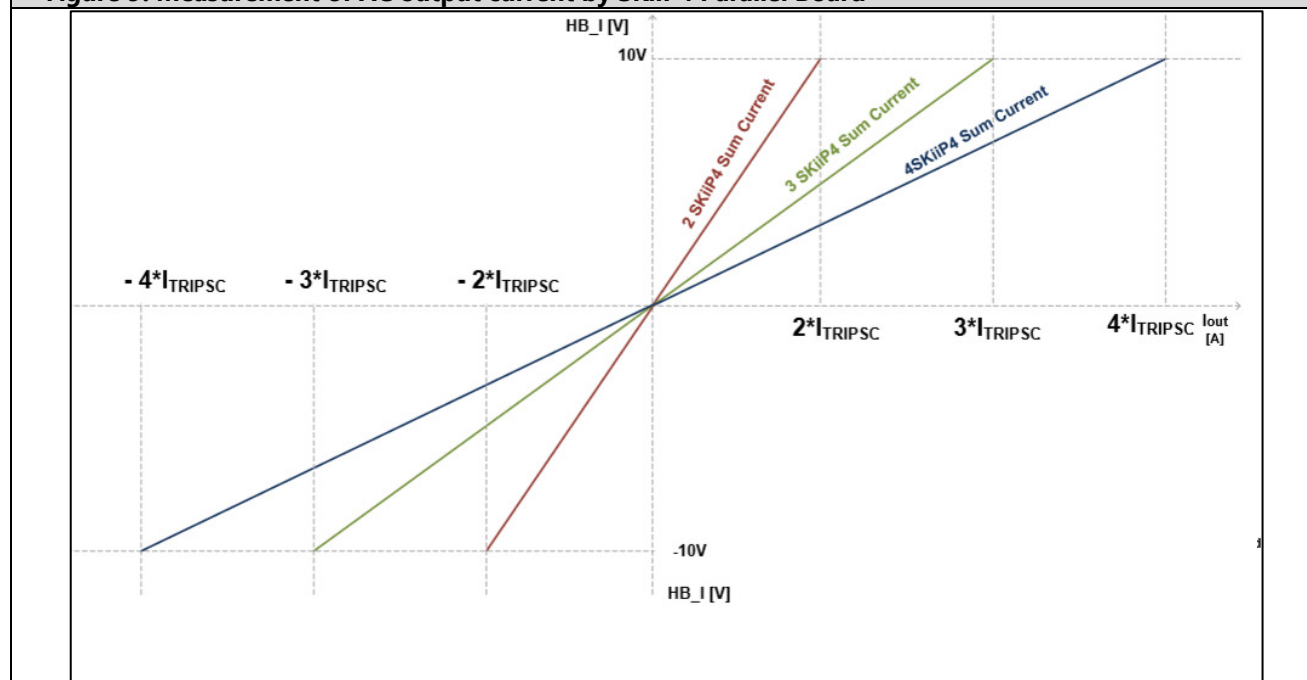
3.4.2 AC output current measurement

The Parallel Board provides a single, consolidated current measurement:

- It sums the output current values from all connected SKiiP4.
- It converts the total summed current into a proportional analog voltage, which is available at the X1 connector.

The controller must then divide this total current value by the number of SKiiPs to determine the average current per module (as shown in Figure 9). The I_{TRIPSC} value for a specific SKiiP4 can be found in its datasheet.

Figure 9: Measurement of AC output current by SKiiP4 Parallel Board



The values provided in Table 6 are specific to the SKiiP4 Parallel Board. For the SKiiP4's own current measurement characteristics, please consult the "Semikron Danfoss Technical Explanation SKiiP4 EN Rev13".

Table 6: Signal characteristics of current measurement for Parallel Board	
Signal characteristics	Value
Output signal	HB_I/HB_I_GND at connector X1
Max output current	5mA
Output voltage range	-10V to +10V (normalized, independent from number of SKiiP4)
Current value per connected SKiiP4	Parallel board for 2 SKiiPs in parallel → HB_I x 0.5 Parallel board for 3 SKiiPs in parallel → HB_I x 0.33 Parallel board for 4 SKiiPs in parallel → HB_I x 0.25
Accuracy of analog signal over full temperature range (ΔI_{OUT} Parallel Board)	+/-1.8%

3.4.3 DC-link voltage measurement

The Parallel Board processes the DC-link voltage signals as follows:

- It receives the individual analog DC-link voltage signals from each SKiiP4.
- It compares all incoming voltage values.
- It provides the single highest (maximum) voltage value to the controller.

This final analog signal U_{DCL} is made available at the X1 connector, and its characteristics are defined in Table 7.

The values provided in Table 7 are specific to the SKiiP4 Parallel Board. For the SKiiP4 own DC-link voltage measurement characteristics, please consult the "Semikron Danfoss Technical Explanation SKiiP4 EN Rev13".

Table 7: signal characteristics of voltage measurement for Parallel Board	
Signal characteristics	Value
Output signal	CMN_DCL/CMN_DCL_GND at connector X1
Max output current	5mA
Output voltage range	0V to 10V
Analog DC-Link voltage signal CMN_DCL @900V	9V for 1200V SKiiP4 6.5V for 1700V SKiiP4
Analog DC-Link voltage signal CMN_DCL @1200V	Not applicable for 1200V SKiiP4 9V for 1700V SKiiP4
Signal bandwidth	Max 4kHz
Accuracy of analog signal over full temperature range	+/-1.6%

3.5 Digital input/output signals

Please refer to "Semikron Danfoss Technical Explanation SKiiP4 EN Rev13".

3.5.1 Synchronization signal for parallel operation

When operating two or more SKiiP4 in parallel connection, the GPIO2 port is used to synchronize the IntelliOff mode for widely balanced current sharing when IntelliOff is activated.

- ! The GPIO2 must be assigned to this functionality before by a command through the CAN interface. Then the ports of all parallel operating SKiiP4 must be connected.

The command through the CAN interface can be made via CANopen tool or direct access, as described in the document "Semikron Danfoss Technical Explanation SKiiP4 CAN Interface V2".

Sub-Index	0
Access type	Read-Write
Description	Enables the parallel mode if the value is written to 1.
Default value	0
Value range	0 – 1
Index	0x3017
Name of variable	Parallel enable
Object code	VAR
Data type	Boolean

How to enable the parallel mode via CAN direct access?

Access this entry with the following CAN-frames:

The request frame:
 Identifier = 600h + Node-ID
 DCL = 8

The response frame:
 Identifier = 580h + Node-ID
 DCL = 8

Example for enabling the parallel mode:

Identifier	Data							
0x62c	22	17	30	0	1	0	0	0
0x5ac	60	17	30	0	0	0	0	0

Example for reading if the parallel mode is enabled or disabled:

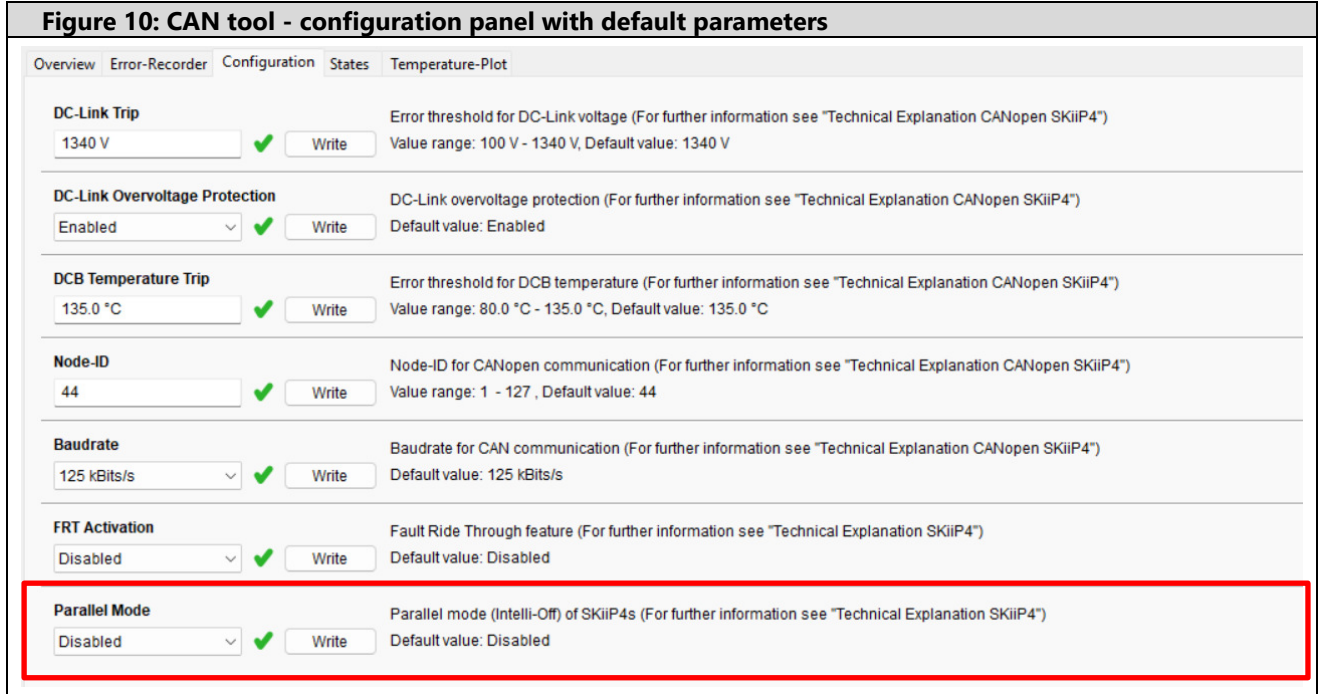
Identifier	Data							
0x62c	40	17	30	0	0	0	0	0
0x5ac	4f	17	30	0	0	0	0	0

The received data is 0x0 which means that the parallel mode is disabled.

How to enable the parallel mode via CANopen tool?

The other option to enable the parallel mode is to use the Semikron-Danfoss CANTool [6].

Figure 10: CAN tool - configuration panel with default parameters

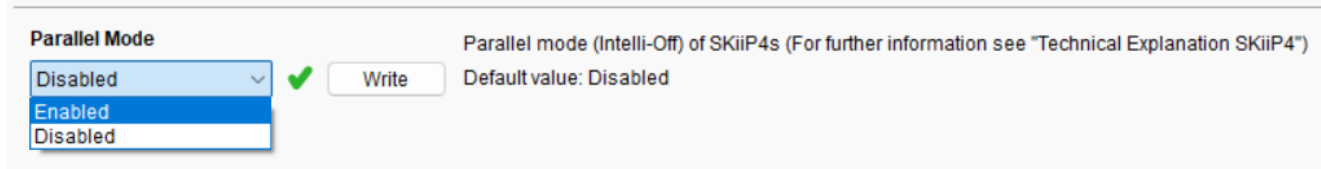


The screenshot shows the 'Configuration' tab of the CAN tool. The 'Parallel Mode' parameter is set to 'Disabled' and is highlighted with a red rectangle. Other parameters include DC-Link Trip (1340 V), DC-Link Overvoltage Protection (Enabled), DCB Temperature Trip (135.0 °C), Node-ID (44), Baudrate (125 kBits/s), and FRT Activation (Disabled).

Parameter	Value	Status	Description
DC-Link Trip	1340 V	✓	Error threshold for DC-Link voltage (For further information see "Technical Explanation CANopen SKiiP4") Value range: 100 V - 1340 V, Default value: 1340 V
DC-Link Overvoltage Protection	Enabled	✓	DC-Link overvoltage protection (For further information see "Technical Explanation CANopen SKiiP4") Default value: Enabled
DCB Temperature Trip	135.0 °C	✓	Error threshold for DCB temperature (For further information see "Technical Explanation CANopen SKiiP4") Value range: 80.0 °C - 135.0 °C, Default value: 135.0 °C
Node-ID	44	✓	Node-ID for CANopen communication (For further information see "Technical Explanation CANopen SKiiP4") Value range: 1 - 127, Default value: 44
Baudrate	125 kBits/s	✓	Baudrate for CAN communication (For further information see "Technical Explanation CANopen SKiiP4") Default value: 125 kBits/s
FRT Activation	Disabled	✓	Fault Ride Through feature (For further information see "Technical Explanation SKiiP4") Default value: Disabled
Parallel Mode	Disabled	✓	Parallel mode (Intelli-Off) of SKiiP4s (For further information see "Technical Explanation SKiiP4") Default value: Disabled

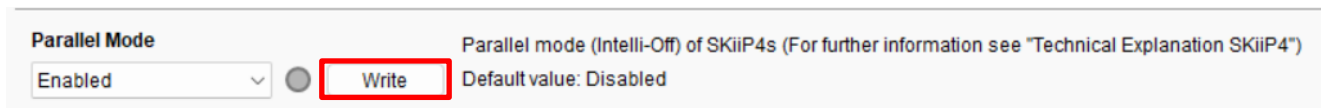
Note: the visual aspect might differ depending on the version of CAN tool used.

Step 1:



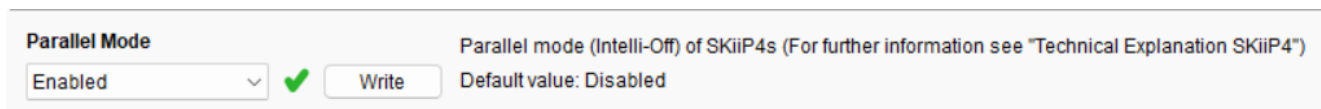
The screenshot shows the 'Parallel Mode' dropdown menu with 'Disabled' selected. The 'Write' button is visible next to it.

Step 2:



The screenshot shows the 'Parallel Mode' dropdown menu with 'Enabled' selected. The 'Write' button is highlighted with a red rectangle.

Step 3: final check

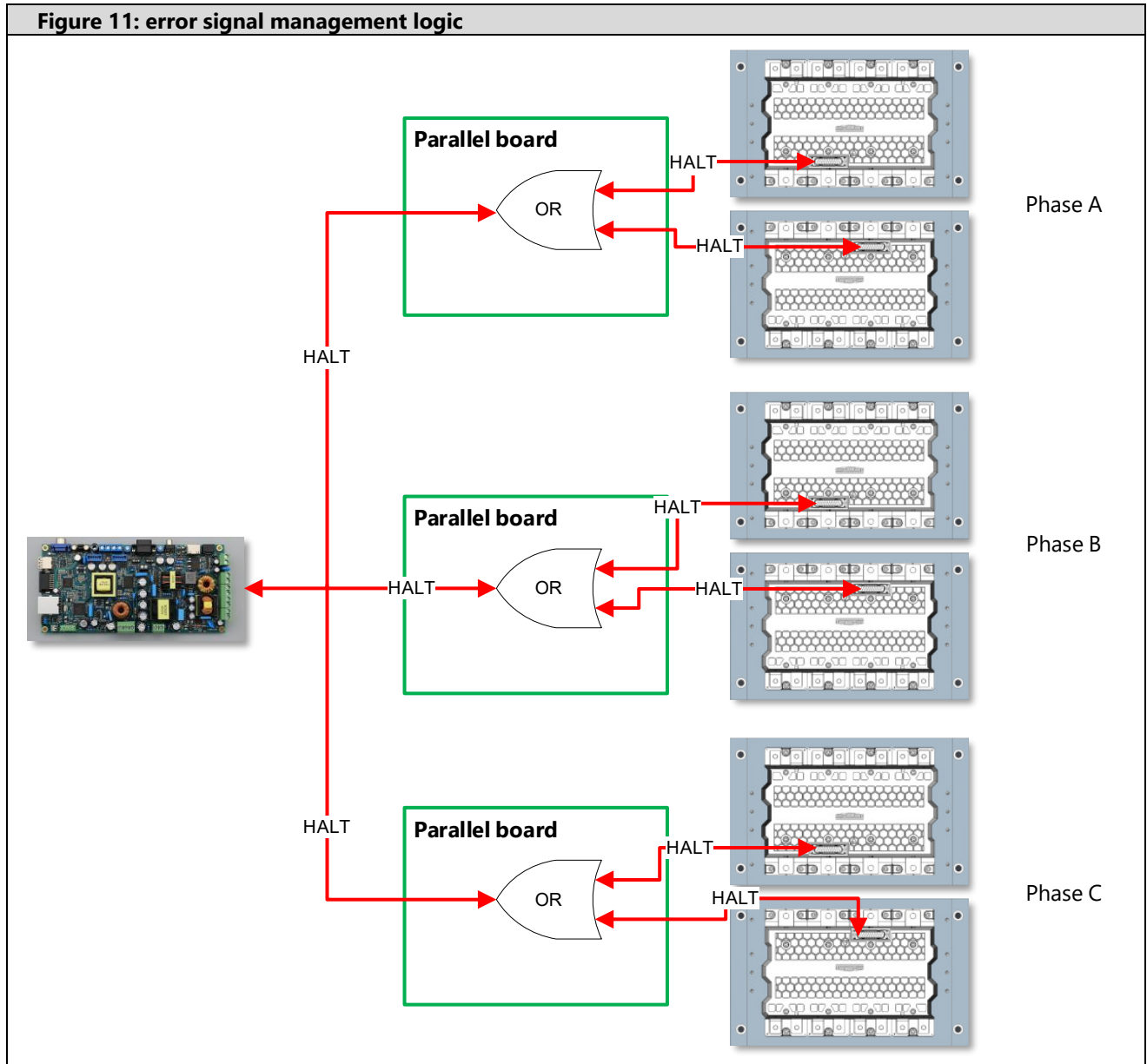


The screenshot shows the 'Parallel Mode' dropdown menu with 'Enabled' selected. The 'Write' button is highlighted with a red rectangle.

3.5.2 Error signal management

The HALT signals of all SKiiP4 in one application shall be connected. The Parallel Board transfers the HALT signals from all connected SKiiP4 to the controller using an OR logic. An error signal from the controller will also stop all the connected SKiiP4.

Figure 11: error signal management logic

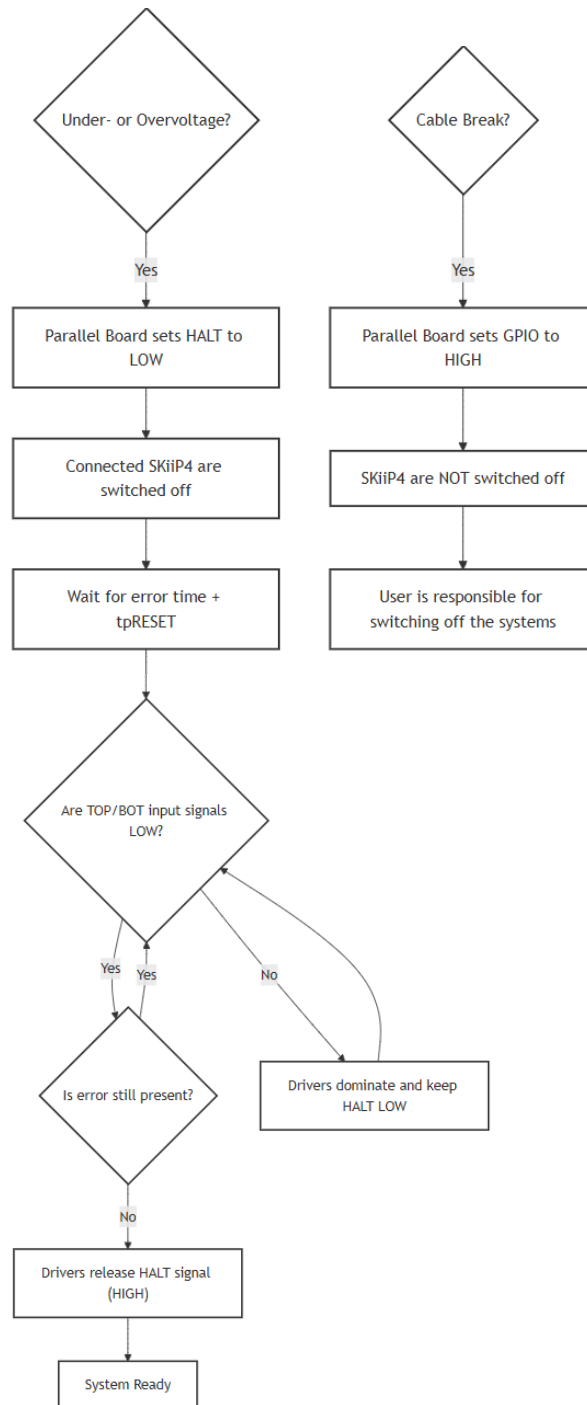


In a paralleled configuration, this is not possible to see which SKiiP set the HALT signal. For this purpose, the CAN-diagnostic interface should be used.

In addition, the Parallel Board has two own failure management features:

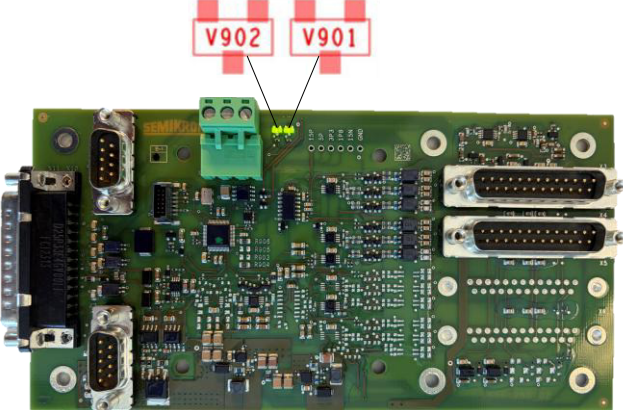
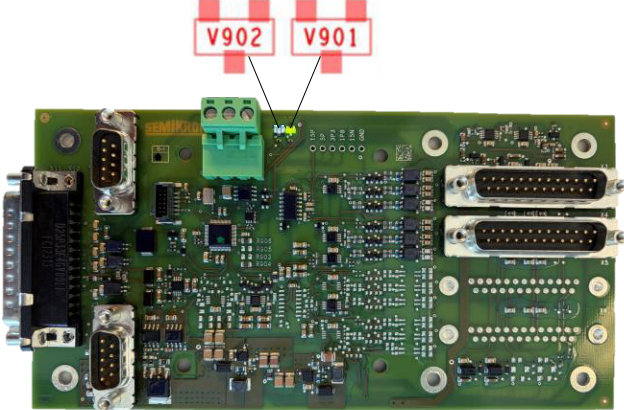
- Monitoring of internal voltages: all internally generated power supplies are monitored to avoid undervoltage and overvoltage.
- Detection of cable break over GPIO1 error signal

The management failure is described in the Figure 12.

Figure 12: Flowchart for management of Parallel Board failures


3.7 Error indication with LED

Two LEDs on the Parallel Board provide error indication. Refer to Figure 14 for their location and the LED state meaning. The error indicated by the LED is an OR-wired HALT signal of the connected SKiiPs.

Figure 14: LED position of the SKiiP4 Parallel Board and LED state meaning			
Error		No error	
V902	V901	V902	V901
Green	Green	OFF	Green
			

Only above listed states are possible in regular operation mode. If some other state is present, there is no supply voltage for the board, or the LED/LEDs are out of functioning.

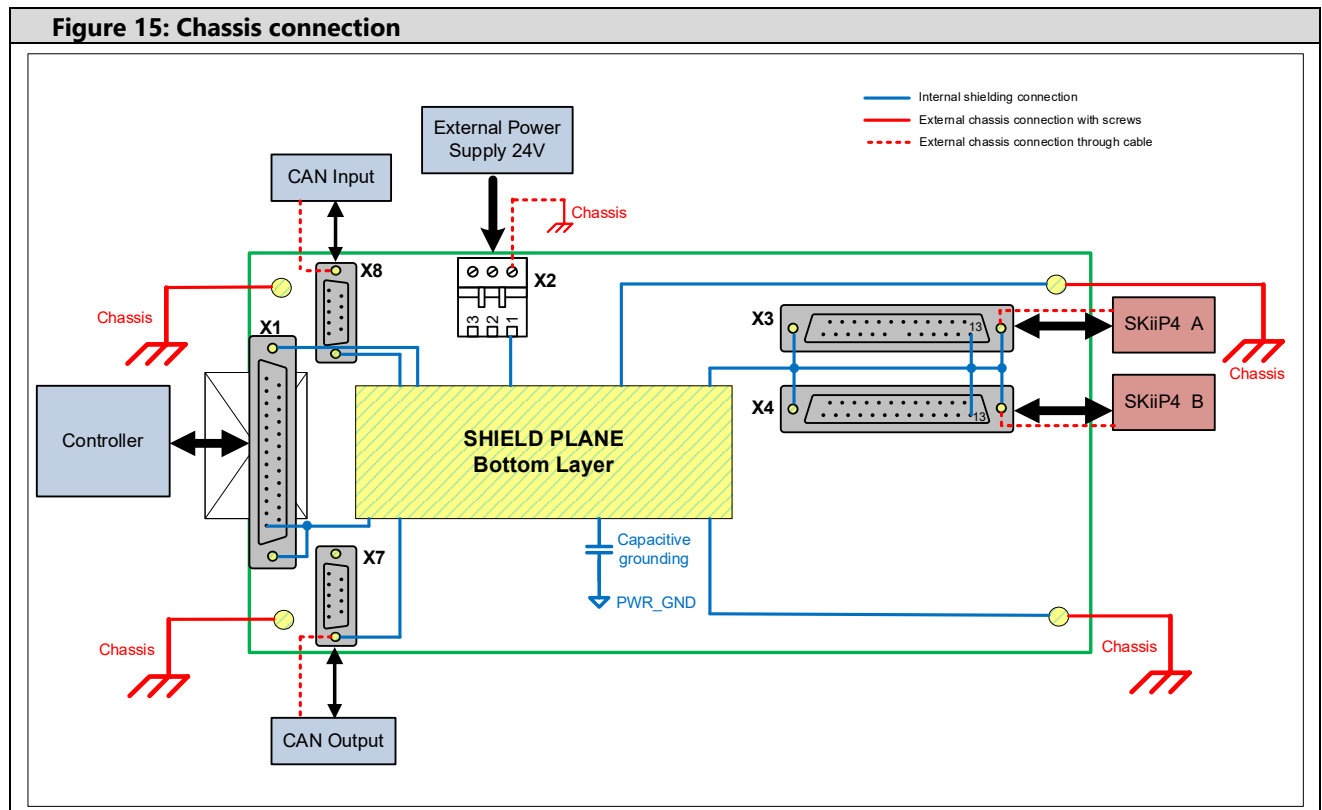
3.8 Shielding concept

For proper shielding, the shields from all D-sub connectors (X1, X3, X4, X5, X6, and X7) are to be centrally merged with the shield plane located within the board. Note that a capacitive connection exists between the SHIELD and the PWR_GND.



The shield level must then be connected to the Chassis/PE. This is achieved by fastening the SKiiP4 Parallel Board to the rear panel's metal frame with four metal screws, which provide the necessary electrical connection. The screws used for this purpose must have a head diameter smaller than 7.7mm.

Figure 15: Chassis connection



4. Frequently Asked Questions

Is it recommended to derate the output current?

Yes, Semikron-Danfoss advises derating the theoretical converter power. A 10% derating in the output current per converter is recommended as an initial guideline. This should be verified by analyzing the current balance between the parallel SKiPs and could be reduced afterwards.

What happens if a SKiP fails in a system using a Parallel Board?

In the event of a failure in one of the parallel SKiPs, the entire system will shut down and remain inoperative until the defective SKiP is replaced.

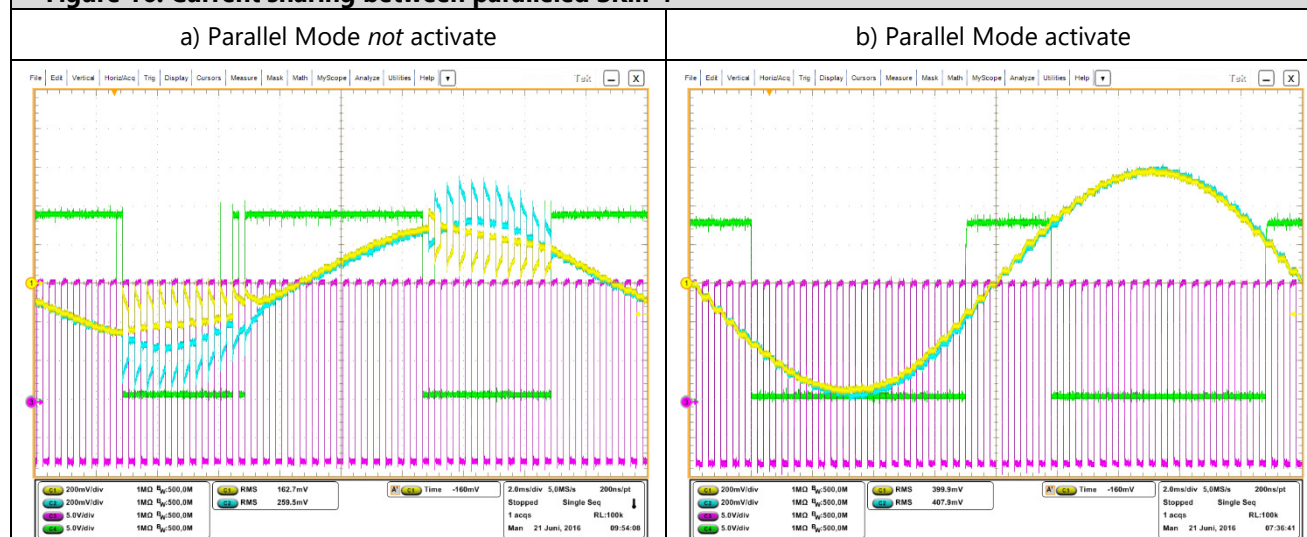
Is it possible to use Fault Ride Through (FRT) function while using the Parallel Boards?

Yes. As described in SKiP4 technical explanation, when FRT mode is activated, an overcurrent trip will never set CMN_HALT to LOW, but all the other failures will.

IntelliOff functionality with Parallel SKiP4 Modules

The IntelliOff function is compatible with SKiP4 modules operating in parallel. The GPIO2 pin synchronizes the IntelliOff mode across modules to achieve balanced current sharing. Refer to Section 3.5.1 for the parallel mode activation procedure required to ensure proper operation.

Figure 16: Current sharing between paralleled SKiP4



How works the short pulse suppression and extension features with a Parallel Board?

The short pulse suppression time is defined as t_{SIS} in Parallel Board datasheet.

Any command signal – ON or OFF - detected at controller interface (X1 connector) that is extremely short (lasting less than t_{SIS}) is automatically identified as noise and is simply ignored. This prevents any disruption from electrical noise.

Sometimes, a legitimate command can be very short. To prevent any confusion, if a command is valid (lasting more than t_{SIS}) but lasts for less than $1\mu s$, the Parallel Board does not just accept it but reinforces it by extending its duration to a full $1\mu s$. This ensures the command at SKiP interface is clear and robust.

Is it acceptable to use cables of different lengths between the Parallel Board and the SKiPs?

Yes, with certain limitations. As a general requirement, the cable length between the parallel board and each SKiP should be limited to a maximum of 3 meters. A length difference of up to 1 meter between the individual cables is acceptable. For applications requiring cable lengths greater than 3 meters, we recommend using a Fiber Optic interface instead.

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Table 9: X8 (CAN input) connector pin assignment	16

Symbols and Terms

Letter Symbol	Term
DBC	Direct Bonded Copper
I_{out}	Output current of a circuit
IPM	Intelligent Power Module
I_{TRIPSC}	SKiiP Overcurrent Trip Level
P/N	Part Number
PWR_GND	
V_{CE}	Collector Emitter Voltage
V_{DC}	DC link voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors"

Errata and feedback

We strive to ensure that this document is accurate and up to date. If you identify any errors, inconsistencies, omissions, or unclear information, please report them to: SKiiP_documentation@danfoss.com

Your feedback is highly appreciated and helps us continuously improve the quality of our documentation.

References

- [1] www.semikron-danfoss.com
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- [6] "Semikron-Danfoss_CAN Tool Quick Start Guide"

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Semikron Danfoss International GmbH
Sigmundstrasse 200, 90431 Nuremberg, Germany
Tel: +49 911 65596663
sales@semikron-danfoss.com, www.semikron-danfoss.com