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<b>Prepared by:</b>	Daniel Prindle
<b>Approved by:</b>	Andreas Giessmann

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## Silicon Carbide Specific Considerations for SKiiP

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### 1. Silicon Carbide SKiiP Introduction

Fourth generation silicon carbide MOSFETs have been introduced into the SKiiP4 product line. The high-performance digital driver of the SKiiP4 enables the introduction of new SiC devices without any interface changes required by the customer. At the time of writing, the following part number has been introduced:

Table 1: New Part Number	
SKiiP2414MB20IF01-4DUHP	2400A rated, 4-bay, half-bridge module

### 2. Performance Differences

As the name suggests, silicon carbide chips are made from a different material than silicon devices and therefore have different properties. These are discussed below:

#### 2.1 Faster switching speeds

The faster switching speeds of SiC enable a considerably higher switching frequency to be used, even for a 2kV IPM. The faster switching speeds also result in higher dv/dt and di/dt values than older SKiiPs, especially for users accustomed to the SKiiP3, for example. Higher dv/dt values may result in higher stress in motor windings and filter components. The dv/dt must be checked in the final application.

#### 2.2 1500VDC capability

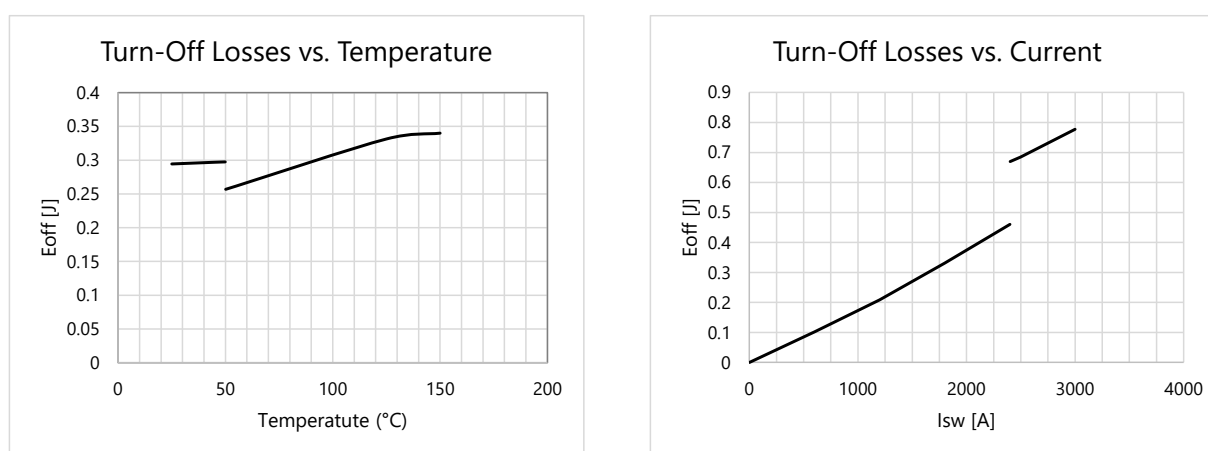
2kV MOSFETs have been selected for the SiC SKiiP, an increase in blocking voltage over the 1700V rated IGBT IPMs. Previously, 1700V devices were limited to 1500V only at low currents to avoid overvoltages, so-called 'Open Circuit 1500V' capability. 2kV rated SiC MOSFETs, however, are 1500V-capable across the whole operating zone, provided that the system stray inductance is kept to a low level. See the respective module datasheet and chapter 4 for more details on this topic.

### 2.3 IntelliOff addition

IntelliOff has been a feature of the 1700V SKiiP4 IPMs for a long time. IntelliOff is an automatic feature of the driver board that uses a higher turn-off gate resistor to limit the overvoltage at high currents. See Section 5.7 of the SKiiP4 Technical Explanation [3] for more details on this feature.

The SiC SKiiP introduces a new condition to IntelliOff. In addition to IntelliOff activating at high currents, this feature is also active for SiC IPMs at low temperatures. This reduces the overvoltage peaks generated during diode turn-off at low temperatures (and therefore low load currents), but enables a higher efficiency at high temperatures and load currents. The crossover point for SiC SKiiPs is at 50°C, as measured by the internal temperature sensor not the junction temperature.

**Figure 1: Switching Losses vs. Temperature and Current**



Conditions:  $V_{DC} = 1200V$ ,  $I_{sw} = 1800A$ ,  $T_j$  Varied

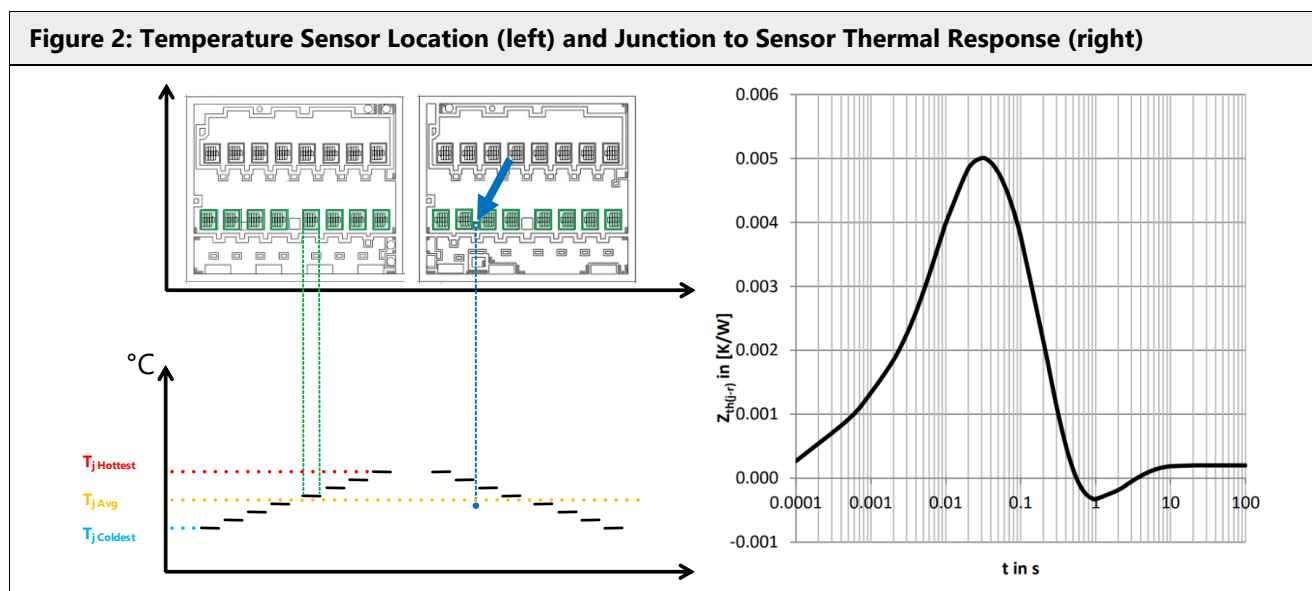
$V_{DC} = 1200V$ ,  $I_{sw}$  Varied,  $T_j = 150^\circ C$

If SiC SKiiP modules are connected in parallel, it is critical to take the following steps to avoid IntelliOff mismatches and poor current sharing between IPMs.

- Enable 'Parallel Mode' via the CAN interface
- Connect the GPIO2 pins of each IPM
- Make sure that the busbar and cooling paths are symmetrical for each module to ensure the same operating conditions for each IPM

### 3. Temperature Feedback

As shown in the figure below, temperature sensor (highlighted in **blue**) is very close to the power chips (MOSFETs in **green**) along with the  $R_{th(j-r)}$  figure from the SKiiP2414MB20IF01-4DUHP datasheet. Note that this is a simplification to explain the behavior of the  $R_{th(j-r)}$  curve. Because the sensor is positioned between two of the hotter chips, it will measure roughly the average junction temperature  $T_{j\text{ Avg}}$  after the system reaches thermal equilibrium.

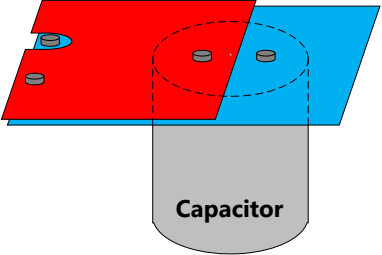
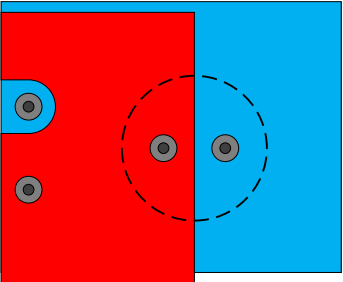
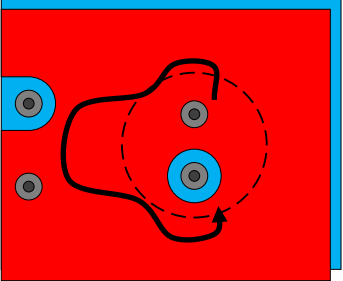
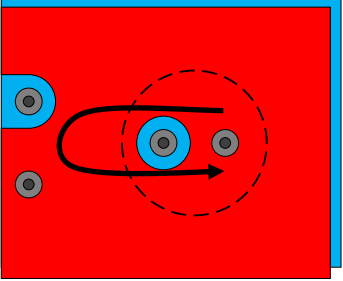
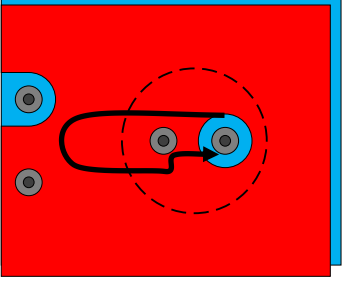


### 4. System Stray Inductance

The higher switching speeds of silicon carbide MOSFETs require a lower stray inductance than typically seen in IGBT systems. If the stray inductance is too high, high voltage overshoots may occur as the device switches off, potentially causing damage to the IPM.

Because the SKiiP is an Intelligent Power Module with an integrated gate driver, the gate resistor values cannot be adjusted to reduce voltage overshoot if the stray inductance is too high. The system stray inductance must be managed during the initial design.

The following tables show some simple improvements that can be made to reduce the system stray inductance to an acceptable level for SiC IPMs. Changing from the 'Bad' design to the 'Best' design results in a roughly 40% reduction in stray inductance, so this aspect is important to a proper SiC system.

Table 2: Effect of capacitor connection on stray inductance		
<p><b>Module Terminals</b></p>  <p><b>Capacitor</b></p>	<p><b>Example</b></p>	<p>This table shows the impact of the capacitor terminal rotation and position on stray inductance.</p>
<p>View from Top</p> 	<p><b>Bad</b></p>	<p>Minimal overlap of upper layer over bottom layer results in very high stray inductance. This kind of design should be avoided. The area for the bolt holes should be kept to a minimum and both layers should be fully overlapping.</p>
	<p><b>OK</b></p>	<p>Fully overlapping layers dramatically reduces stray inductance.</p> <p>However, installing the capacitor parallel to the module terminals results in a wider loop, resulting in higher inductance relative to the designs below.</p>
	<p><b>Better</b></p>	<p>By having the terminals perpendicular to the DC terminals, the loop area is significantly reduced.</p>
	<p><b>Best</b></p>	<p>The terminal of the upper layer (farther from the capacitor) should be closer to the DC terminals of the module. Minimizing the distance the farther layer carries current will minimize the loop area. The positive and negative polarity is not relevant, but rather the layers and their distance to the capacitor.</p>

The table below shows different ways of connecting the capacitor bank to the DC terminals of the SKiiP. The traditional 'finger' style of connection results in a high stray inductance is not recommended. DC connections with maximum overlap should be implemented.

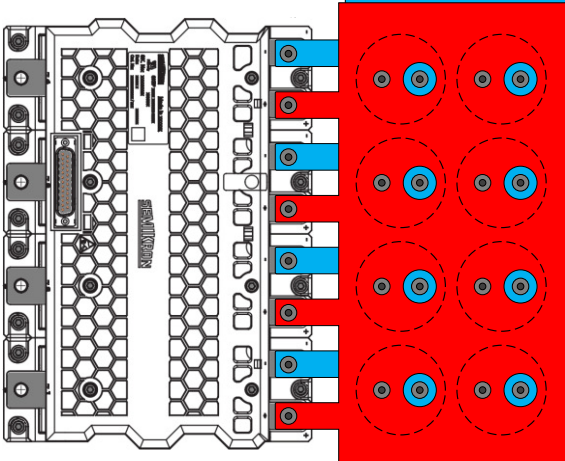

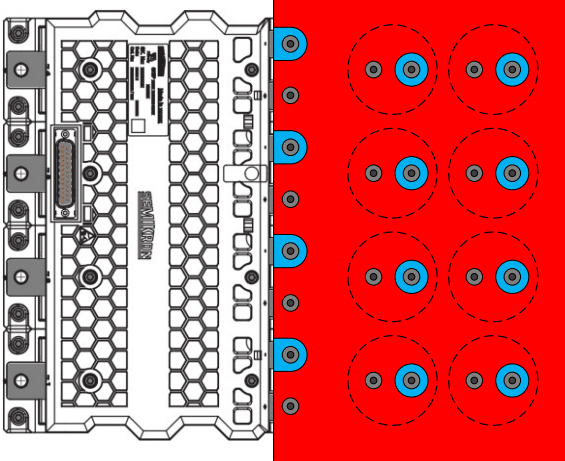
Table 3: Effect of DC terminal connections on stray inductance (view from top)		
	<b>Bad</b>	<p>'Finger' type busbar connections like this have previously been acceptable for IGBT-based system. However, this will result in too high of a stray inductance for a SiC MOSFET SKiiP.</p> <p>This kind of design is not recommended.</p>
	<b>Better</b>	<p>The addition of shunting busbars that connect the individual DC+ and DC- terminals may be helpful in reducing the stray inductance of an existing design without major rework.</p> <p>Design files for these shunting busbars are available from Semikron Danfoss to assist in system development.</p>
	<b>Best</b>	<p>By extending the busbar layers fully to the DC terminals of the SKiiP, the stray inductance can be reduced.</p> <p>Snubber capacitors may not be necessary if the final stray inductance is low enough to avoid large overvoltage spikes.</p> <p>Mechanical stress by misaligned bolt holes can cause damage to the module. The bolt holes must be large enough to compensate for differences in mechanical tolerances.</p>

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### Symbols and Terms

Letter Symbol	Term
di/dt, dv/dt	Rate of change in current (i) or voltage (v) in time
IPM	Intelligent Power Module
$R_{th(j-r)}$	Thermal resistance from junction to temperature sensor
SiC	Silicon Carbide
$T_j$	Junction temperature

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2].

### References

- [1] [www.semikron-danfoss.com](http://www.semikron-danfoss.com)
- [2] A. Wintrich et al., "Application Manual Power Semiconductors", 3rd edition, Semikron Danfoss International GmbH, [www.semikron-danfoss.com](http://www.semikron-danfoss.com)
- [3] A. Schiller, "Technical Explanation SKiiP4", Semikron Danfoss International GmbH 2024, [www.semikron-danfoss.com](http://www.semikron-danfoss.com)
- [4] D. Prindle et al., "Silicon Carbide Power Modules", Application Note An 24-001 – rev01, Semikron Danfoss, [www.semikron-danfoss.com](http://www.semikron-danfoss.com)

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Semikron Danfoss International GmbH  
Sigmundstrasse 200, 90431 Nuremberg, Germany  
Tel: +49 911 65596663  
sales@semikron-danfoss.com, www.semikron-danfoss.com