Application Note
AN 25-001

SEMIKRON DANFOSS

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Prepared by:	Jürgen Engstler
Approved by:	Dr. Uwe Schilling

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Paralleling Thyristor Modules

1. Introduction

In high-power applications, thyristors are connected in parallel because a single device cannot meet the required current and power ratings. In recent years, a new trend has emerged: instead of using a single high-power thyristor, several smaller thyristor modules are employed for economic reasons. High-power thyristors are typically implemented as disk cells in press-pack housings, whereas smaller thyristors are based on standard rectangular chips with a corner or central gate, packaged in standard soldered housings with bond-wire top connections. This packaging technology is also used for IGBT and diode modules, which are produced in high volumes. As a result, the same production lines and, in many cases, the same housings can be utilized across these device types.
Small thyristor modules provide a superior cost-to-output current ratio than traditional disk cell thyristors and are available from a wider range of suppliers.
These modules facilitate a platform strategy, allowing for the creation of scalable power inverter families. By paralleling modules, designers can easily create different power classes. This approach streamlines inventory by reducing part numbers and increases purchasing volume.

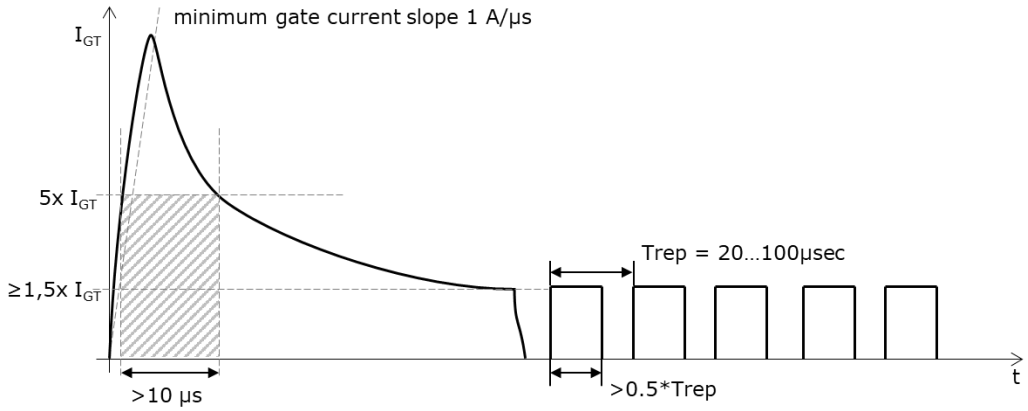
Improvements in thyristor production during the last decades reduced manufacturing tolerances, especially in the on-state voltage (V_T), and enable the reliable performance of paralleled modules.

2. Crucial Points Considering Dynamic Current Sharing

2.1 Recommendations for trigger circuits in parallel operation

To ensure reliable and fast triggering of a thyristor, it is recommended to apply a gate trigger pulse with an amplitude of at least five times I_{GT} for at least 10 µs and a rise rate of $di_{GT}/dt \geq 1\,A/\mu s$. Only under these conditions are the datasheet values for $(di/dt)_{cr}$ and t_{GD} valid.
Furthermore, to guarantee secure thyristor ignition, it is advisable to apply a train of trigger pulses to the gate, as illustrated in Figure 1. The train of trigger pulses should continue at least until the load current reaches the latching current of the thyristor. Preferably, the trigger pulses should be maintained throughout the entire conduction phase of the thyristor, as this ensures that a thyristor, which has been inadvertently turned off—particularly at low load currents—will resume conduction. Further details about triggering can be found in [5].

Figure 1: Gate trigger current for a "pulse train" or "fence" triggering



The same applies to thyristors connected in parallel, except that for n parallel thyristors, a trigger pulse with an amplitude of at least $n \times 5 \times I_{GT}$ must be applied. In other words, the triggering equipment must be capable of supplying at least n times the trigger current required for a single thyristor.

The minimum gate trigger current for different thyristor sizes typically ranges between 150 mA and 300 mA; a larger thyristor does not necessarily require a proportionally higher I_{GT}. For example, the SKKT 570 has an I_{GT} of 200 mA, while the SKKT 162 requires 150 mA. In this case a triggering device designed for a single SKKT 570 is not sufficient to drive two or more SKKT 162 in parallel replacing the SKKT 570.
Either a triggering device capable of delivering higher currents must be used, or—as is often done in practice—each thyristor in the parallel arrangement should be provided with its own dedicated trigger circuit.
If a single central gate trigger transformer is used, it is important to place an appropriate resistor in series with each gate and to ensure that the leads to each gate are as equal in length as possible. For a central gate trigger transformer, we recommend designing the current capability to at least $110\% \times n \times I_{GT}$ to compensate for tolerances in gate trigger voltages.

2.2 Impact of paralleling on critical $(di/dt)_{cr}$

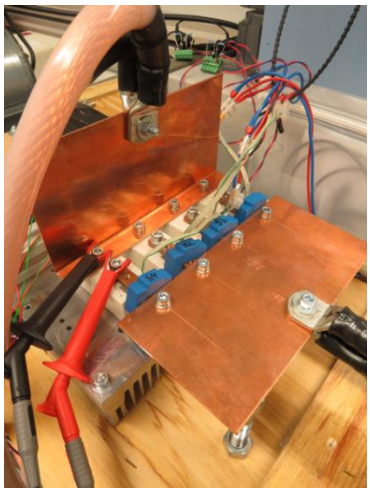
Under ideal conditions, the $(di/dt)_{cr}$ ratings of individual thyristors connected in parallel could be summed. In practice, however, a perfectly symmetrical current distribution at the instant of turn-on cannot be guaranteed. For this reason, when designing with parallel thyristors, the $(di/dt)_{cr}$ rating of a single device should be used as the limiting value.
In mains-powered applications, where several smaller thyristors are used to replace a single larger device, this consideration is generally not critical. Large thyristors do not inherently have higher $(di/dt)_{cr}$ ratings than smaller ones. For example, the SKET 801 has a $(di/dt)_{cr}$ of 200 A/µs, identical to that of the SKKT 162.
In applications where parallel connection is specifically intended to achieve a higher $(di/dt)_{cr}$, the design must be carefully evaluated. If necessary, additional inductors should be added to each parallel branch to promote current sharing and ensure symmetrical operation during turn-on.

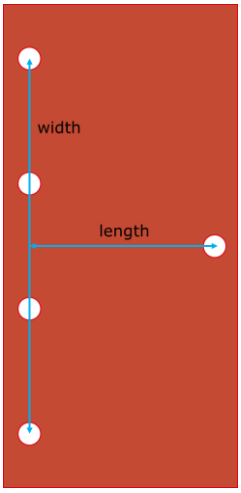
3. Crucial Points Considering Static Current Sharing

3.1 Recommendations for symmetrical circuit design

When designing a system with parallel devices the circuit layout should be symmetrical as possible. The length and cross-section of busbars connecting each device to a common contact should be equal. The same applies for the connections between the gate driver circuits and the devices. Ideally, all parasitic resistances should be identical in every parallel branch.
In the literature elaborate arrangements are proposed to reach this ideal. Like busbars in Christmas tree shape or circular mounting of thyristors with a round plate on top and the cable mounted in the middle.
The empirical experience is, that it is sufficient to use seamless metal plates with a width to length ratio of 3:2 and connect the grid or load cable in the middle (Figure 2). To avoid collisions e.g. with gate interfaces the plates can be bend.

Figure 2: Example busbar





It is crucial that the contact surfaces are flat and free from corrosion layers. If necessary, they have to be cleaned and corrosion layers removed. The contact screws have to be tightened using a controlled torque. The goal is to achieve minimal and equal contact resistances in each branch.

3.2 Recommendations for heatsink design

Parallel thyristor modules should be mounted on the same heatsink with a small spacing of approximately 10 mm between them. This arrangement thermally couples the modules and reduces the risk of current sharing degradation caused by temperature effects on the forward conduction characteristics.

3.3 Impact of V_T tolerances based on production statistics

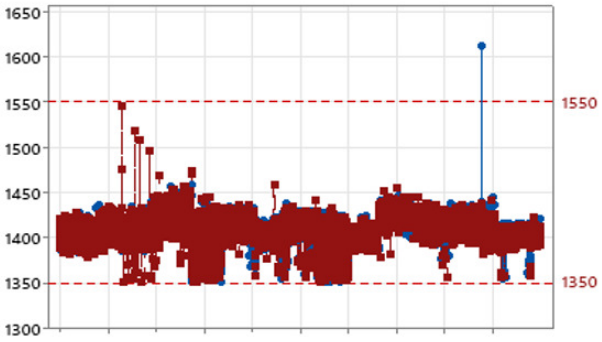
Of all device parameters, the on-state voltage (V_T) tolerance has the most significant impact on current sharing.

Usually, a worst-case analysis relies on the minimum and maximum on-state characteristic values from the datasheet. This approach necessitates a derating of 20-30% or even more, depending on the number of parallel thyristors. However, such a substantial current reduction not only makes parallel operation economically unviable but is also unnecessary in practice. While a worst-case combination is theoretically possible, its statistical probability is exceedingly low.

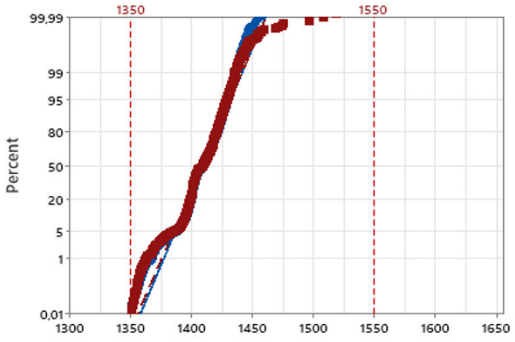
Therefore, this section examines the expected current imbalances using actual V_T statistics from production end of line (EOL) measurements. The analysis is performed with SKKT162 devices, but the methodology can be applied to other thyristor modules as well.

The distribution of the SKKT162 V_T values (Figure 3) can be described by a normal distribution with a standard deviation σ of 14 mV. Evaluations of V_T measurements for various thyristor modules from the SD portfolio over long production periods show standard deviations of $\sigma < 15$ mV, while individual production lots often exhibit standard deviations below 10 mV.

Figure 3: SKKT 162 measurement data EOL 50.000 modules over 2 years, 428 batches



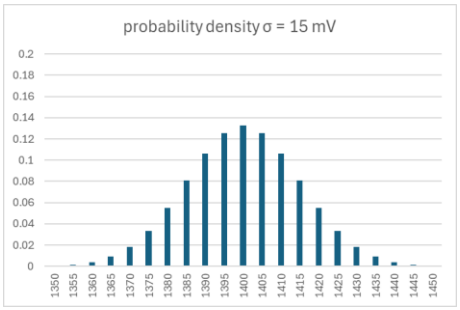
V_T measurements over time



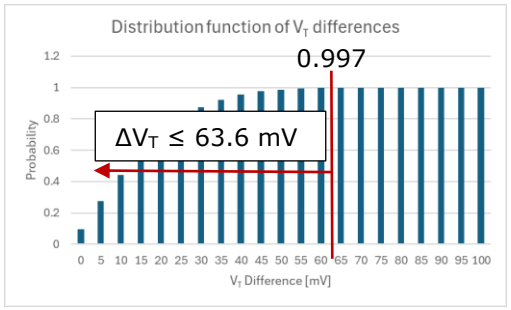
Probability plot

To describe the influence of the V_T value distribution on current sharing in parallel operation, a brief excursion into statistics is necessary. A normal distribution with $\sigma = 15$ mV and a mean value of 1400 mV is assumed. For use in a Monte Carlo analysis, this normal distribution is divided into 5 mV classes (Figure 4 left).

Figure 4: Ideal standard distribution and result of Monte Carlo Analysis



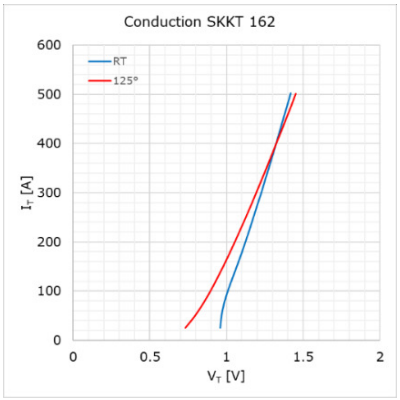
Ideal standard distribution

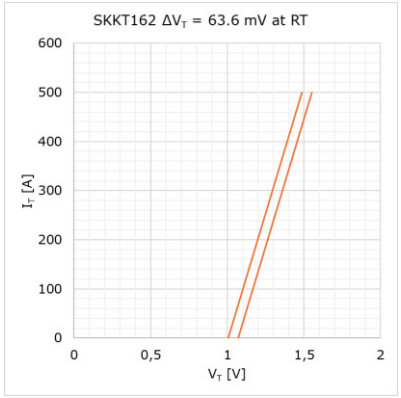


Result Monte Carlo Analysis 2 thyristors parallel

In the Monte Carlo analysis for two thyristors connected in parallel, random pairs are formed from two voltage classes. The asymmetry in current sharing is determined by the difference between the two voltage classes. The result of the Monte Carlo analysis shows that 99.7% of the pairs exhibit a voltage difference ΔV_T of 63.6 mV or less (Figure 4 right). This significantly reduces the current-sharing asymmetry compared to a worst-case analysis based on min-max datasheet limits.
Monte Carlo analyses were also carried out for three and four randomly selected thyristors, and the maximum voltage difference was determined within which 99.7% of the 3-device (113.6 mV) and 4-device (165 mV) groups fall. These maximum voltage differences were then used in the simulation model to determine derating factors.

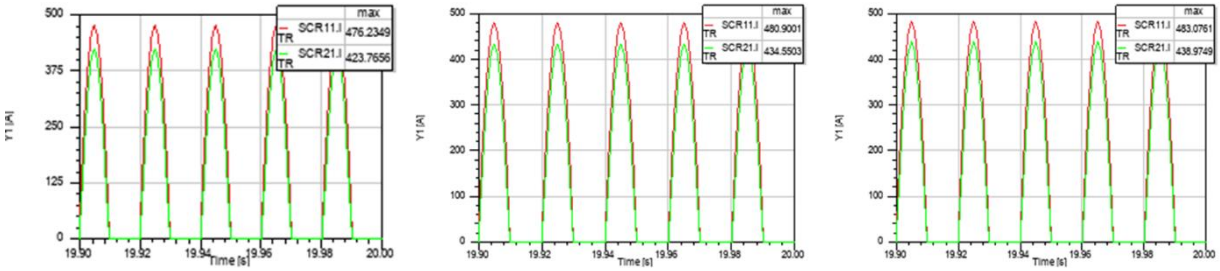
Figure 5: Conduction characteristic SKKT 162 and linear approximation ΔV_T = 63.6 mV





For the parallel connection simulation, linear approximations representing the upper and lower limits of the V_T characteristic were applied (Figure 5 right). The simulation model incorporates a thermal model of the power modules and a heatsink. The calculated junction temperature is fed back into the semiconductor model, ensuring that the temperature dependence (Figure 5 left) of the forward characteristic is accurately reflected in the simulation results.
Simulations were carried out for the parallel operation of 2, 3, and 4 SKKT162 devices in W3C configuration. In these scenarios, one device was set to operate at the lower V_T limit, while the remaining devices were set to the upper limit, corresponding to a voltage difference of 63.6 mV in case of two thyristors in parallel. The model is parameterized so that, under conditions of symmetrical current sharing, the junction temperature of all thyristors reaches 115 °C.

Figure 6: Simulation results for 2,3 and 4 SKKT 162 in parallel based on statistic approach



2 parallel derating 0,92 | 3 parallel derating 0,91 | 4 parallel derating 0,9

The diagrams show the current profile without derating applied.

A significant reduction in the required derating is achieved. In the statistical approach, for four thyristors connected in parallel, it is sufficient to reduce the total current to $\mathbf{0.9 \times 4 \times I_{TAV}}$ for keeping T_{vj} of all thyristors below the target value of 115°C.

99.7% of the random pairings fall within the determined voltage difference. Statistically, larger deviations can occur in 3 out of 1000 cases. However, this does not mean that such cases will lead to an immediate failure. It merely indicates that, in these instances, individual thyristors may reach a higher junction temperature, which, in the worst case, could lead to a reduction of service life.
The same calculations were performed for two additional module classes, yielding identical results. Therefore, these findings can be transferred to other thyristors in module packages. A more detailed description of the statistical approach can be found in [3].

In practice, it is advisable to request the V_T distribution for the respective module from Semikron Danfoss and, taking into account the cooling conditions of the application, calculate the static asymmetry caused by V_T tolerances. Often a higher junction temperature of the device, that takes more current, is not critical, because there is enough headroom in the cooling system and the junction temperature of the device is below the max. permissible junction temperature.

4. Test Results Parallel Operation of Thyristor Halfbridge Modules

A dedicated test rig was developed for the SKKT 162 thyristor series, enabling parallel operation of up to four modules under a 50 Hz sinusoidal half-wave supply. The setup supports both single half-wave tests at ambient temperature and continuous 50 Hz operation with forced air cooling, allowing evaluation of thermal behavior under sustained load conditions.

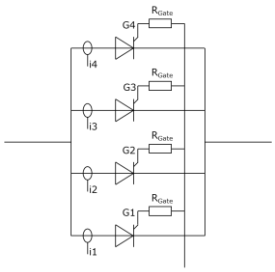
SKKT 162 devices manufactured in 2012, 2015, 2018, and 2025 were tested. For each production year, four modules were selected and connected in parallel. A mixed configuration combining devices from all four production years was also evaluated.

Additional test configurations were implemented for four SKKT 323 modules in parallel and two SKKT 570 modules in parallel.

4.1 Measurement setup for investigation on parallel thyristors

Figure 7: Test Set up for 4 SKKT 162 in parallel

Top view



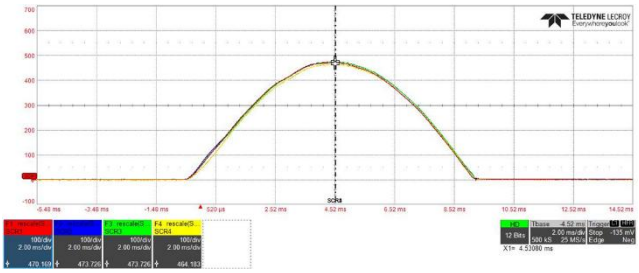
Test circuit

Copper busbars with a width-to-length ratio of 3:2 were used for the electrical connections.

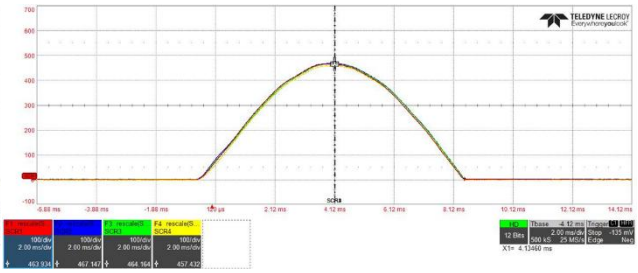
4.2 Measurements 4 parallel SKKT 162

In the tests, single pulses were measured at ambient temperature, as well as continuous pulses for 10 minutes at a repetition frequency of 50 Hz. After 10 minutes of operation, the case temperature T_C reached approximately 70 °C.

Figure 8: 4 SKKT 162 of production year 2012

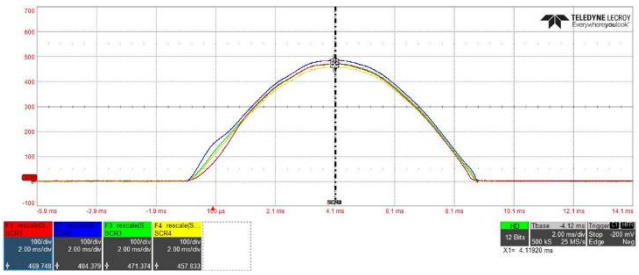


Single pulse

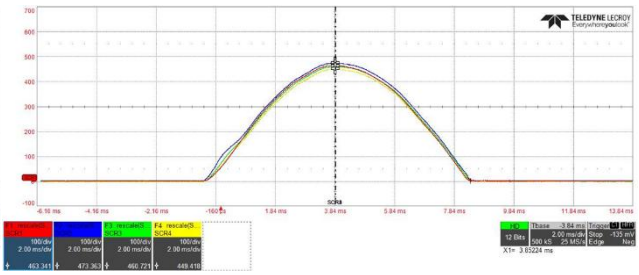


10 min continuous pulses

4 SKKT 162 of production year 2015

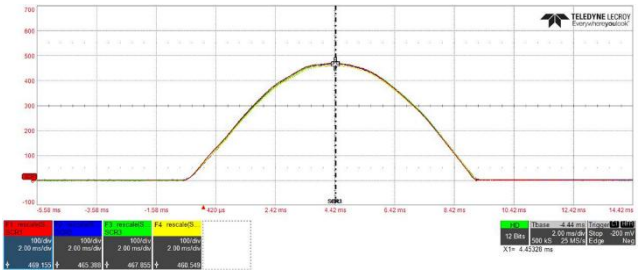


Single pulse

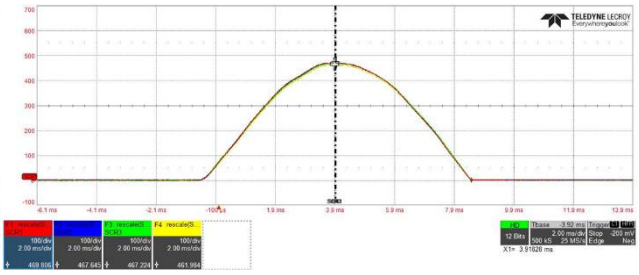


10 min continuous pulses

4 SKKT 162 of production year 2018

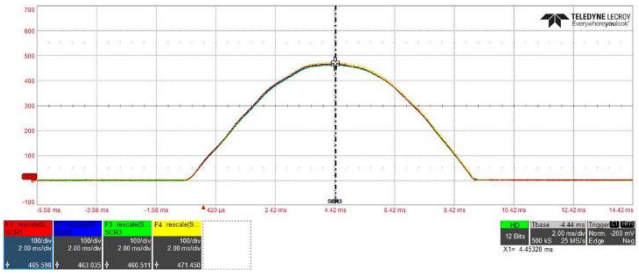


Single pulse

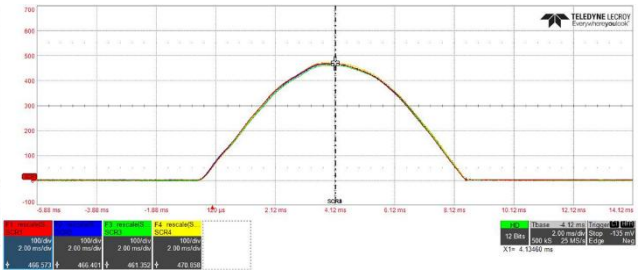


10 min continuous pulses

4 SKKT 162 of production year 2025



Single pulse



10 min continuous pulses

4 SKKT 162 of production years 2012, 2015, 2018 and 2025

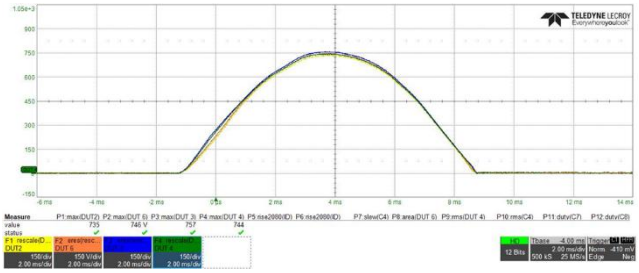
Single pulse

The measured peak values deviated by less than 3 % from the theoretical mean value. As the temperature increased, the already small differences between the currents became even smaller. No thermal drift between the devices was observed.

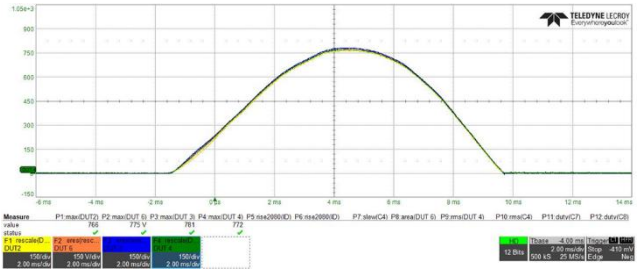
4.3 Measurements 4 parallel SKKT 323

From a batch of six SKKT 323 devices, four were selected in which three V_T measurements were at the upper end of the range and one V_T measurement was at the lower end.
During testing, single pulses were measured at ambient temperature, as well as continuous pulses for 3 minutes at a repetition frequency of 50 Hz. After 3 minutes of operation, the case temperature T_C reached 83 °C.

Figure 9: 4 SKKT 323 parallel



Single pulse



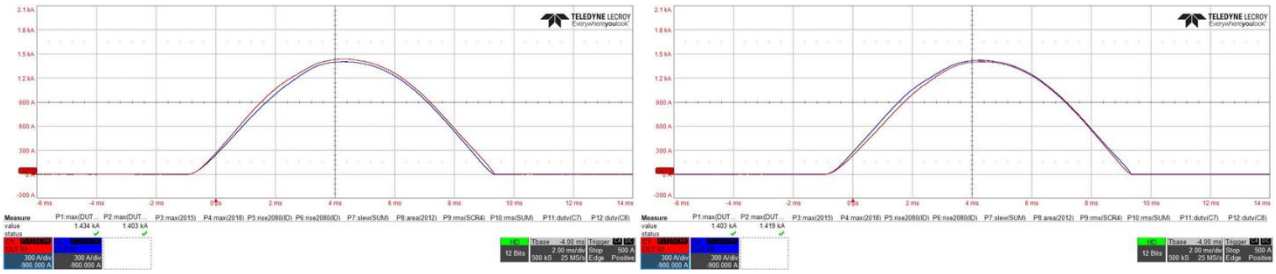
3 min continuos pulses

The measured peak values deviated by less than 1.5 % from the theoretical mean value. As the temperature increased, the already small differences between the currents became even smaller. No thermal drift between the devices was observed.

4.4 Measurements 2 parallel SKKT 570

From a batch of six SKKT 570 devices, all possible pair combinations were tested in parallel operation. Figure 10 shows the results for two of these pairings as examples; all other combinations exhibited similar behavior.

Figure 10: pair of SKKT 570 parallel



Single pulse DUT01 and DUT02 parallel | Single pulse DUT01 and DUT06 parallel

The measured peak values deviated by less than 1.5 % from the theoretical mean value.

5. Summary and Conclusion

The presented investigations have proven that there is no showstopper for parallel operation of thyristor modules in mains applications.
The dominant factor influencing current sharing between thyristors is the variation in on-state voltage V_T. Advances in manufacturing technology have substantially reduced V_T tolerances compared with devices manufactured in the 1960s and 1970s. As a result, recommendations and instructional practices concerning parallel operation—originally derived from experiences with earlier generations of thyristors—should be critically reassessed.

In the present work, a statistical approach is introduced based on V_T measurements from the production of modern thyristors. This approach yields a realistic current derating of approximately 10% for thyristors connected in parallel. For the specific application case, it is recommended to calculate the junction temperatures based on the V_T distribution of the thyristors, taking the cooling system into account. In many cases, derating can be omitted, as elevated junction temperatures in individual thyristors—caused by current asymmetries—can be compensated by the headroom in the junction temperatures.

The following design aspects are important for paralleling thyristor modules in mains applications:

- Mechanically symmetric layout with thyristor modules coupled electrically as symmetrical as possible.
- Thermally symmetric layout with thermally coupled thyristor modules to reduce temperature differences.
- Appropriate gate trigger with synchronous, steep and high current pulses (min. 110% of the sum of required gate trigger currents of each individual thyristor, continuous sequence of trigger pulses during the whole conduction period to force a proper retriggering of turned off thyristors)
- Separate gate resistors for each module to enhance/enforce gate current symmetry.

To ensure thyristor modules are suitable for parallel connection without providing End-of-Line measurement data, Semikron Danfoss can provide selected thyristor module types with an optional tighter V_T specification. If these special thyristor module types are required, please contact a Semikron Danfoss sales representative.

Symbols and Terms

Letter Symbol	Term
V_G	Gate voltage
I_G	Gate current
V_{GT}	Gate trigger voltage
I_{GT}	Gate trigger current
I_L	Latching current
I_H	Hold current
V_T	On-state voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2].

References

[1] www.semikron-danfoss.com
[2] A. Wintrich, U. Nicolai, A. Giessmann, S. Berberich, "Application Manual Power Semiconductors", 3rd edition, edited by Semikron Danfoss International
[3] U. Scheuermann, "Statistical Evaluation of Current Imbalance in Parallel Devices", Proc. PCIM Europe 2016, 691-697, ISBN 978-3-8007-4186-1.
[4] IEC 60747-6:2016-04, Ed. 3.0 Semiconductor Devices – Part 6: Discrete devices -Thyristors
[5] AN 18-002 Thyristor Triggering and Protection of Diodes and Thyristors

IMPORTANT INFORMATION AND WARNINGS

Semikron Danfoss International GmbH
Sigmundstrasse 200, 90431 Nuremberg, Germany
Tel: +49 911 65596663
sales@semikron-danfoss.com, www.semikron-danfoss.com